

# System Reset Monolithic IC PST600

## Outline

This IC operates in a variety of CPU systems and other logic systems by detecting power supply voltage, so that the system can be reset accurately when power is turned on or when power is momentarily cut. PST572 and others perform the same function as does this series, but this IC is a low reset type system resetting IC which follows load current so that circuit current flow increases for ON, and has low current consumption for both ON and OFF.

## Features

1. Follows load current so that circuit current flow increases for ON, and has low current consumption for both ON and OFF.
2. Low operating limit voltage
3. Hysteresis voltage provided in detection voltage
4. The following 10 ranks of detection voltages are available.

No load :  $I_{CCL}=7\mu A$  typ.;  $I_{CCH}=5\mu A$  typ.

0.65V typ.

50mV typ.

PST600	C : 4.5V typ.	H : 3.1V typ.
	D : 4.2V typ.	I : 2.9V typ.
	E : 3.9V typ.	J : 2.7V typ.
	F : 3.6V typ.	K : 2.5V typ.
	G : 3.3V typ.	L : 2.3V typ.

## Package

MMP-3A (PST600□M)

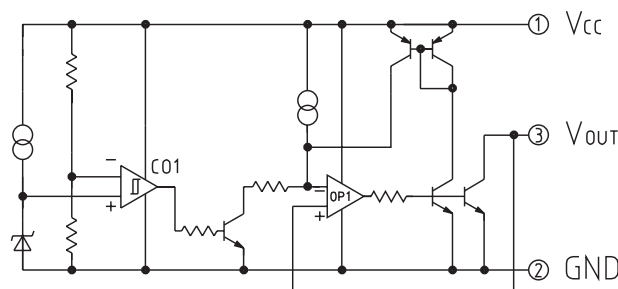
TO-92A (PST600□)

\*□ contains detection voltage rank.

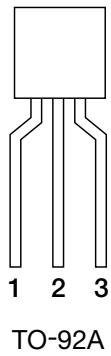
## Applications

1. Microcomputers, CPU, MPU reset circuits
2. Logic circuit reset circuits
3. Battery voltage check circuits
4. Back-up power supply switching circuits
5. Level detection circuits

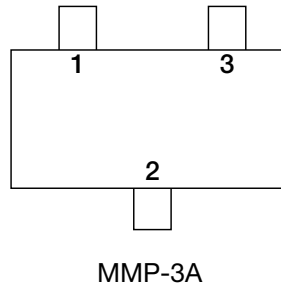
## Equivalent Circuit



Pin Assignment



1	V <sub>CC</sub>
2	GND
3	V <sub>OUT</sub>



1	V <sub>CC</sub>
2	GND
3	V <sub>OUT</sub>

Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Ratings	Units
Storage temperature	T <sub>STG</sub>	-40~+125	°C
Operating temperature	T <sub>OPR</sub>	-20~+75	°C
Power supply voltage	V <sub>CC</sub> max.	-0.3~10	V
Allowable loss	P <sub>d</sub>	200 (MMP-3A) 300 (TO-92A)	mW

Electrical Characteristics (Ta=25°C) (unless otherwise indicated resistance unit is Ω)

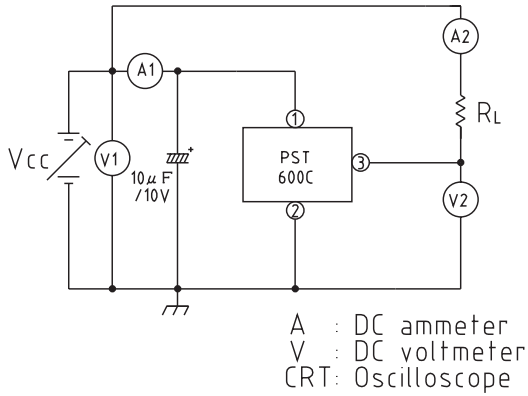
Item	Symbol	Measurement circuit	Measurement conditions	Min.	Typ.	Max.	Units	
Detection voltage	V <sub>s</sub>	1	R <sub>L</sub> =470 V <sub>OL</sub> ≤ 0.4V V <sub>CC</sub> =H→L	PST600C	4.3	4.5	4.7	V
				PST600D	4.0	4.2	4.4	
				PST600E	3.7	3.9	4.1	
				PST600F	3.4	3.6	3.8	
				PST600G	3.1	3.3	3.5	
				PST600H	2.9	3.1	3.3	
				PST600I	2.75	2.90	3.05	
				PST600J	2.55	2.70	2.85	
				PST600K	2.35	2.50	2.65	
				PST600L	2.15	2.30	2.45	
Hysteresis voltage	ΔV <sub>s</sub>	1	R <sub>L</sub> =470, V <sub>CC</sub> =L→H→L	30	50	100	mV	
Detection voltage temperature coefficient	V <sub>s</sub> /ΔT	1	R <sub>L</sub> =470, Ta=-20°C~+75°C		±0.01		%/°C	
Low level output voltage	V <sub>OL</sub>	1	V <sub>CC</sub> =V <sub>s</sub> min. -0.05V, R <sub>L</sub> =470		0.3	0.4	V	
Output leak current	I <sub>OH</sub>	1	V <sub>CC</sub> =10V			±0.1	μA	
Circuit current for ON	I <sub>CC</sub> L	1	V <sub>CC</sub> =V <sub>s</sub> min. -0.05V	I <sub>OL</sub> =0mA		7	14	μA
				I <sub>OL</sub> =8mA		50	130	
Circuit current for OFF	I <sub>CC</sub> H	1	V <sub>CC</sub> =V <sub>s</sub> typ./0.85V, R <sub>L</sub> =∞		5	10	μA	
H transmission delay time	t <sub>PLH</sub>	2	R <sub>L</sub> =4.7k, C <sub>L</sub> =100pF *1	20	40	80	μS	
L transmission delay time	t <sub>PHL</sub>	2	R <sub>L</sub> =4.7k, C <sub>L</sub> =100pF *1	10	20	40	μS	
Operating limit voltage	V <sub>op</sub> L	1	R <sub>L</sub> =4.7k, V <sub>OL</sub> ≤ 0.4V		0.65	0.85	V	
Output current 1 for ON	I <sub>OL</sub> 1	1	V <sub>CC</sub> =V <sub>s</sub> min. -0.05V, R <sub>L</sub> =0	8			mA	
Output current 2 for ON	I <sub>OL</sub> 2	1	Ta=-20°C~+75°C, R <sub>L</sub> =0 *2	6			mA	

\*1 t<sub>PLH</sub> : V<sub>CC</sub>= (V<sub>s</sub> typ. -0.4V) → (V<sub>s</sub> typ.+0.4V), t<sub>PHL</sub> : V<sub>CC</sub>= (V<sub>s</sub> typ.+0.4V) → (V<sub>s</sub> typ.-0.4V)

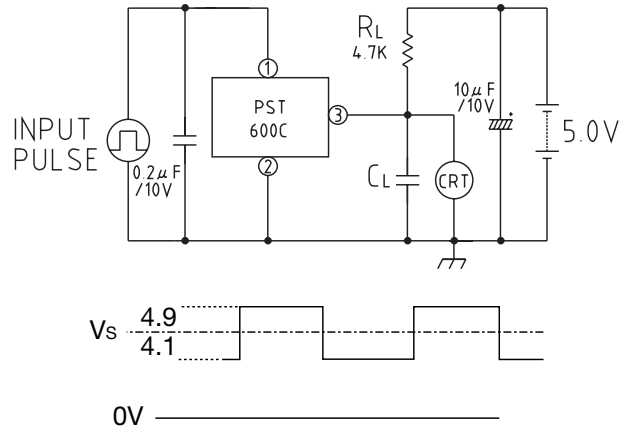
\*2 V<sub>CC</sub>=V<sub>s</sub> min. -0.15V

Measurement Circuit

[1]



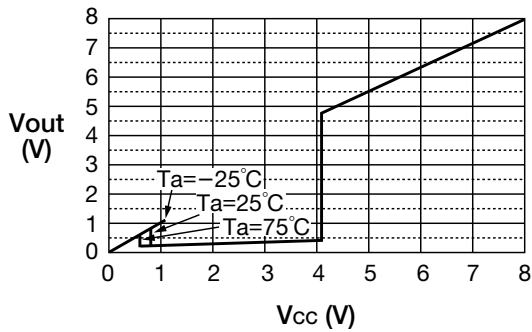
[2]



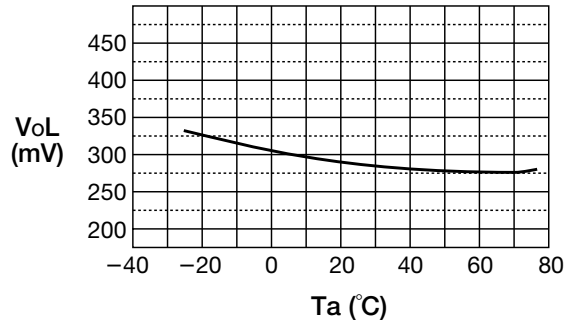
\* The input model is an example of PST600C (MMP-3P).

Characteristics (PST600C is used as the representative model for characteristics examples.)

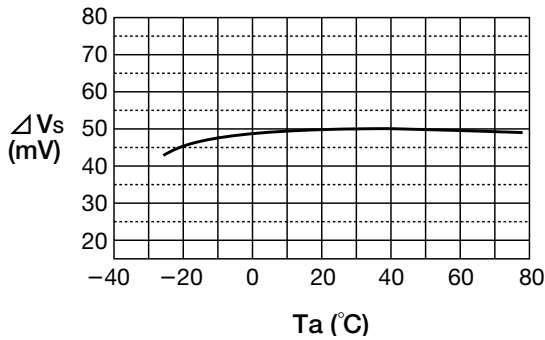
■  $V_{CC}$  vs.  $V_{OUT}$



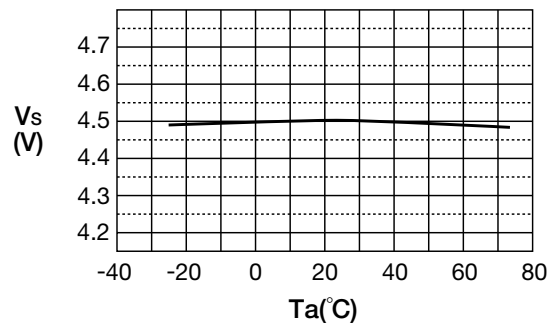
■  $V_{OL}$  vs.  $T_a$



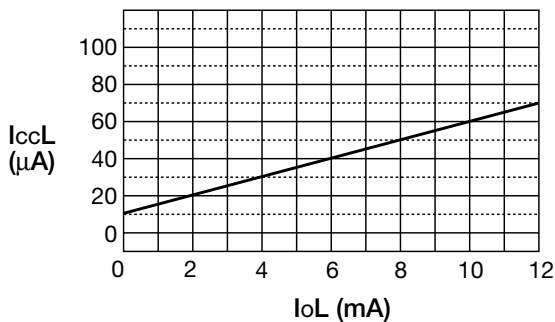
■  $\Delta V_s$  vs.  $T_a$



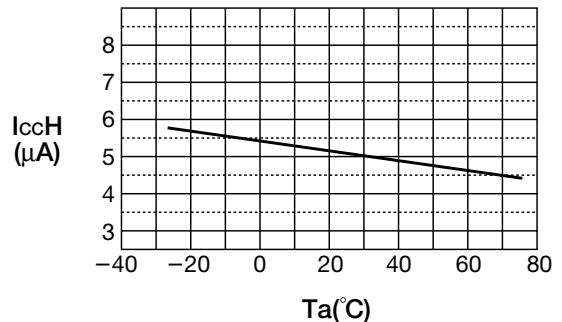
■  $V_s$  vs.  $T_a$



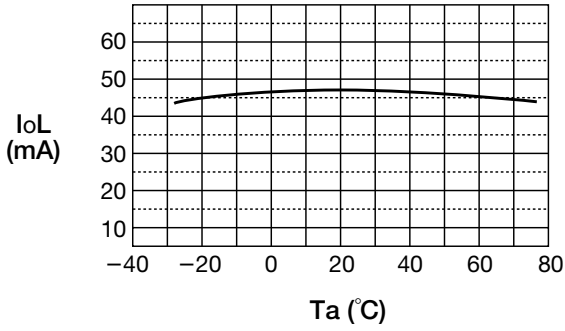
■  $I_{cCL}$  vs.  $I_{oL}$



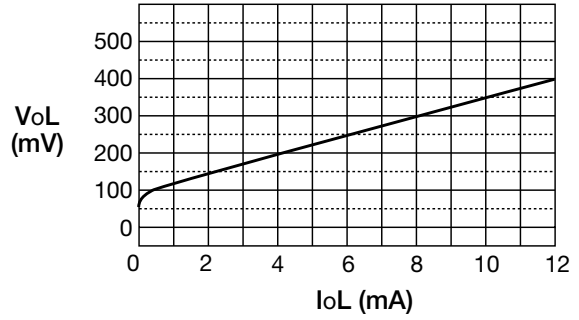
■  $I_{cCH}$  vs.  $T_a$



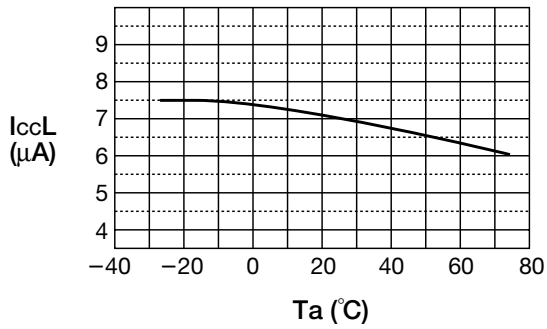
IoL vs. Ta



VoL vs. IoL

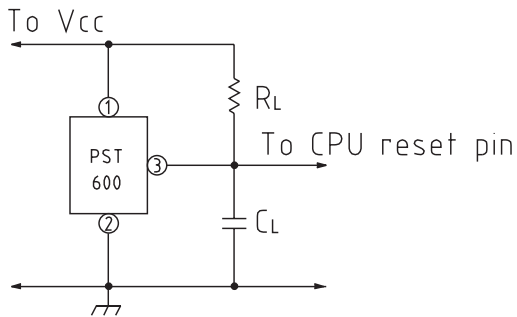


IccL (IoL=0mA) vs. Ta



Application Circuits

1. Normal hard reset



Delay Time (tPLH)

$$t_{PLH} \approx C_L \times R_L \times \left[ \ln \frac{V_{CC}}{V_{CC} - (V_{S_{CPU}} + 0.2)} \right] + 0.040 \text{ (mS)}$$

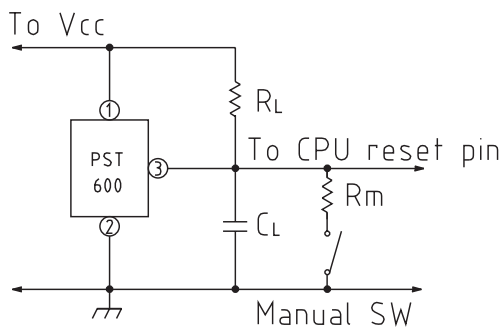
$C_L$  :  $\mu\text{F}$        $V_{S_{CPU}}$  : CPU, MPU reset threshold voltage

$R_L$  :  $\text{k}\Omega$

Voltage : V

Note : When  $V_{CC}$  line impedance is high, connect a capacitor between IC Pins 1 and 2.

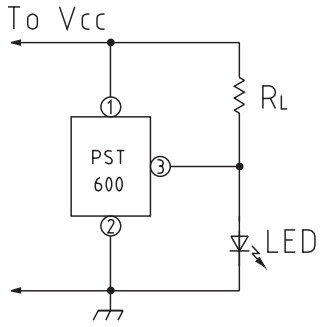
2. Manual Reset



Note : Prevent Manual SW chattering by using  $R_L$ ,  $C_L$  and  $R_m$ .  $R_m$  setting conditions are as follows :  $R_m \leq 1/20 R_L$

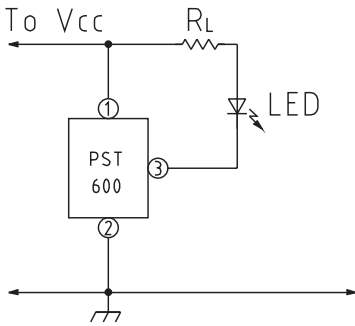
Note : When  $V_{CC}$  line impedance is high, connect a capacitor between IC Pins 1 and 2.

3. Battery Checker (LED ON for High voltage)



Note : When V<sub>CC</sub> line impedance is high, connect a capacitor between IC Pins 1 and 2.

4. Battery Checker (LED ON for Low voltage)



Note : When V<sub>CC</sub> line impedance is high, connect a capacitor between IC Pins 1 and 2.

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