

FEATURES

Excellent Sonic Characteristics
 High Output Drive Capability
 5.2 nV/ $\sqrt{\text{Hz}}$ Equivalent Input Noise @ 1 kHz
 0.001% THD+N ($V_o = 2.5 \text{ V p-p}$ @ 1 kHz)
 3.5 MHz Gain Bandwidth
 Unity-Gain Stable
 Low Cost

APPLICATIONS

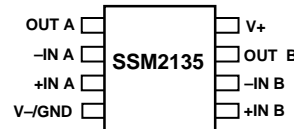
Multimedia Audio Systems
 Microphone Preamplifier
 Headphone Driver
 Differential Line Receiver
 Balanced Line Driver
 Audio ADC Input Buffer
 Audio DAC I-V Converter and Filter
 Pseudo-Ground Generator

GENERAL DESCRIPTION

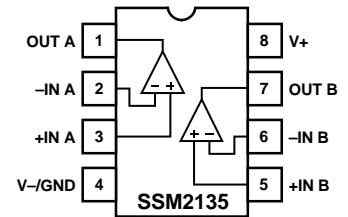
The SSM2135 Dual Audio Operational Amplifier permits excellent performance in portable or low power audio systems, with an operating supply range of +4 V to +36 V or $\pm 2 \text{ V}$ to $\pm 18 \text{ V}$. The unity gain stable device has very low voltage noise of 4.7 nV/ $\sqrt{\text{Hz}}$, and total harmonic distortion plus noise below 0.01% over normal signal levels and loads. Such characteristics are enhanced by wide output swing and load drive capability. A unique output stage* permits output swing approaching the rail

PIN CONNECTIONS

8-Lead Narrow-Body SOIC (S Suffix)



8-Lead Epoxy DIP (P-Suffix)



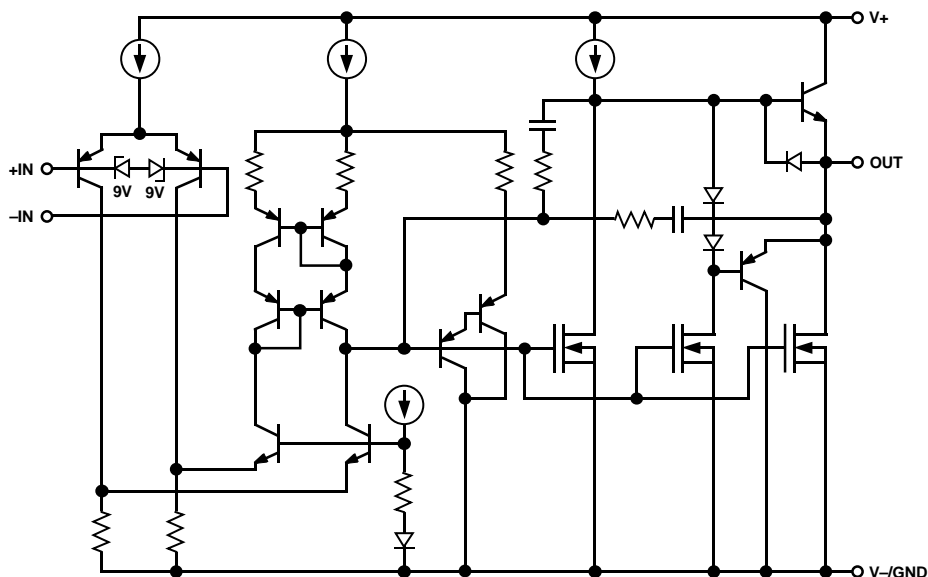
under moderate load conditions. Under severe loading, the SSM2135 still maintains a wide output swing with ultralow distortion.

Particularly well suited for computer audio systems and portable digital audio units, the SSM2135 can perform preamplification, headphone and speaker driving, and balanced line driving and receiving. Additionally, the device is ideal for input signal conditioning in single-supply sigma-delta analog-to-digital converter subsystems such as the AD1878/AD1879.

The SSM2135 is available in 8-lead plastic DIP and SOIC packages, and is guaranteed for operation over the extended industrial temperature range of -40°C to $+85^\circ\text{C}$.

*Protected by U. S. Patent No. 5,146,181.

FUNCTIONAL BLOCK DIAGRAM



REV. D

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SSM2135–SPECIFICATIONS ($V_S = +5\text{ V}$, $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ unless otherwise noted. Typical specifications apply at $T_A = +25^\circ\text{C}$.)

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|-------------------------------|----------|--|---------------|----------------|-----------------|------------------------------|
| AUDIO PERFORMANCE | | | | | | |
| Voltage Noise Density | e_n | $f = 1\text{ kHz}$ | | 5.2 | | $\text{nV}/\sqrt{\text{Hz}}$ |
| Current Noise Density | i_n | $f = 1\text{ kHz}$ | | 0.5 | | $\text{pA}/\sqrt{\text{Hz}}$ |
| Signal-To-Noise Ratio | SNR | 20 Hz to 20 kHz, 0 dBu = 0.775 V rms | | 121 | | dBu |
| Headroom | HR | Clip Point = 1% THD+N, $f = 1\text{ kHz}$, $R_L = 10\text{ k}\Omega$ | | 5.3 | | dBu |
| Total Harmonic Distortion | THD+N | $A_V = +1$, $V_O = 1\text{ V p-p}$, $f = 1\text{ kHz}$, 80 kHz LPF $R_L = 10\text{ k}\Omega$ $R_L = 32\ \Omega$ | | 0.003 0.005 | | % % |
| DYNAMIC PERFORMANCE | | | | | | |
| Slew Rate | SR | $R_L = 2\text{ k}\Omega$, $T_A = +25^\circ\text{C}$ | 0.6 | 0.9 | | $\text{V}/\mu\text{s}$ |
| Gain Bandwidth Product | GBW | | | 3.5 | | MHz |
| Settling Time | t_S | to 0.1%, 2 V Step | | 5.8 | | μs |
| INPUT CHARACTERISTICS | | | | | | |
| Input Voltage Range | V_{CM} | | 0 | | +4.0 | V |
| Input Offset Voltage | V_{OS} | $V_{OUT} = 2\text{ V}$ | | 0.2 | 2.0 | mV |
| Input Bias Current | I_B | $V_{CM} = 0\text{ V}$, $V_{OUT} = 2\text{ V}$ | | 300 | 750 | nA |
| Input Offset Current | I_{OS} | $V_{CM} = 0\text{ V}$, $V_{OUT} = 2\text{ V}$ | | | 50 | nA |
| Differential Input Impedance | Z_{IN} | | | 4 | | $\text{M}\Omega$ |
| Common-Mode Rejection | CMR | $0\text{ V} \leq V_{CM} \leq 4\text{ V}$, $f = \text{dc}$ | 87 | 112 | | dB |
| Large Signal Voltage Gain | A_{VO} | $0.01\text{ V} \leq V_{OUT} \leq 3.9\text{ V}$, $R_L = 600\ \Omega$ | 2 | | | $\text{V}/\mu\text{V}$ |
| OUTPUT CHARACTERISTICS | | | | | | |
| Output Voltage Swing High | V_{OH} | $R_L = 100\text{ k}\Omega$ $R_L = 600\ \Omega$ | 4.1 3.9 | | | V V |
| Output Voltage Swing Low | V_{OL} | $R_L = 100\text{ k}\Omega$ $R_L = 600\ \Omega$ | | | 3.5 3.0 | mV mV |
| Short Circuit Current Limit | I_{SC} | | | ± 30 | | mA |
| POWER SUPPLY | | | | | | |
| Supply Voltage Range | V_S | Single Supply Dual Supply | +4 ± 2 | | +36 ± 18 | V V |
| Power Supply Rejection Ratio | PSRR | $V_S = +4\text{ V}$ to +6 V, $f = \text{dc}$ | 90 | 120 | | dB |
| Supply Current | I_{SY} | $V_{OUT} = 2.0\text{ V}$, No Load $V_S = +5\text{ V}$ $V_S = \pm 18\text{ V}$, $V_{OUT} = 0\text{ V}$, No Load | | 2.8 3.7 | 6.0 7.6 | mA mA |

ABSOLUTE MAXIMUM RATINGS

| | |
|--------------------------------------|---|
| Supply Voltage | |
| Single Supply | +36 V |
| Dual Supply | $\pm 18\text{ V}$ |
| Input Voltage | $\pm V_S$ |
| Differential Input Voltage | 10 V |
| Output Short Circuit Duration | Indefinite |
| Storage Temperature Range | -65°C to $+150^\circ\text{C}$ |
| Operating Temperature Range | -40°C to $+85^\circ\text{C}$ |
| Junction Temperature Range (T_J) | -65°C to $+150^\circ\text{C}$ |
| Lead Temperature (Soldering, 60 sec) | $+300^\circ\text{C}$ |

ESD RATINGS

| | |
|------------------------|-------|
| 883 (Human Body) Model | 1 kV |
| EIAJ Model | 175 V |

THERMAL CHARACTERISTICS

Thermal Resistance¹

| | | |
|--------------------|---------------|---------|
| 8-Lead Plastic DIP | θ_{JA} | 103°C/W |
| | θ_{JC} | 43°C/W |
| 8-Lead SOIC | θ_{JA} | 158°C/W |
| | θ_{JC} | 43°C/W |

¹ θ_{JA} is specified for worst case conditions, i.e., θ_{JA} is specified for device in socket for P-DIP and device soldered in circuit board for SOIC package.

ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option |
|----------|--|---------------------|----------------|
| SSM2135P | -40°C to $+85^\circ\text{C}$ | 8-Lead Plastic DIP | N-8 |
| SSM2135S | -40°C to $+85^\circ\text{C}$ | 8-Lead SOIC | SO-8 |

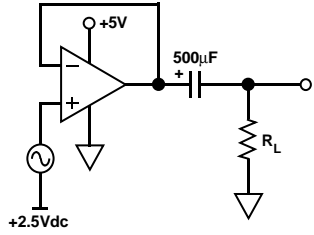


Figure 1. Test Circuit for Figures 2-4

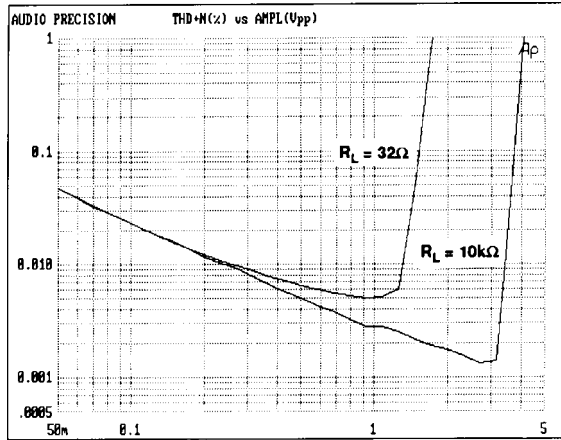


Figure 2. THD+N vs. Amplitude (See Test Circuit; $A_V = +1$, $V_S = +5V$, $f = 1kHz$, with 80 kHz Low-Pass Filter)

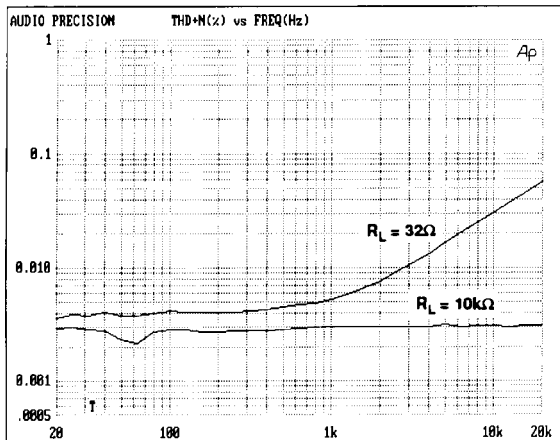


Figure 3. THD+N vs. Frequency (See Test Circuit; $A_V = +1$, $V_{IN} = 1V p-p$, with 80 kHz Low-Pass Filter)

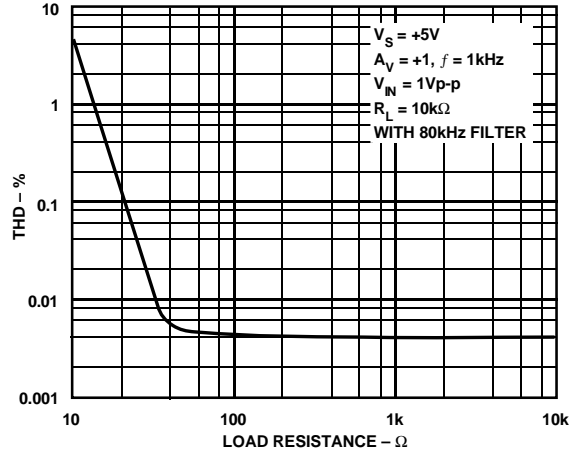


Figure 4. THD+N vs. Load (See Test Circuit)

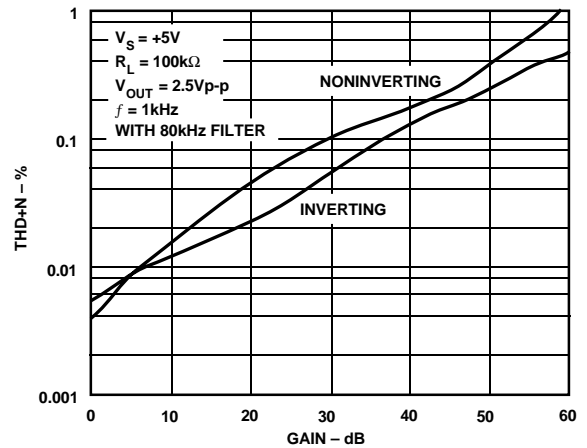


Figure 5. THD+N vs. Gain

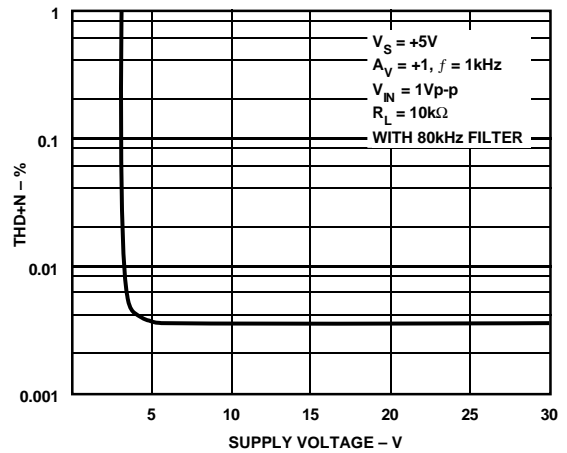


Figure 6. THD+N vs. Supply Voltage

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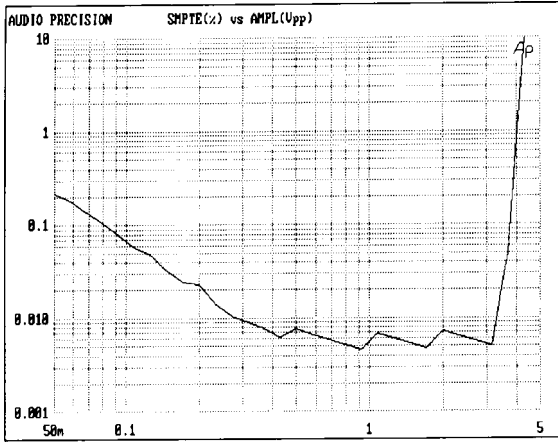


Figure 7. SMPTE Intermodulation Distortion ($A_V = +1$, $V_S = +5\text{ V}$, $f = 1\text{ kHz}$, $R_L = 10\text{ k}\Omega$)

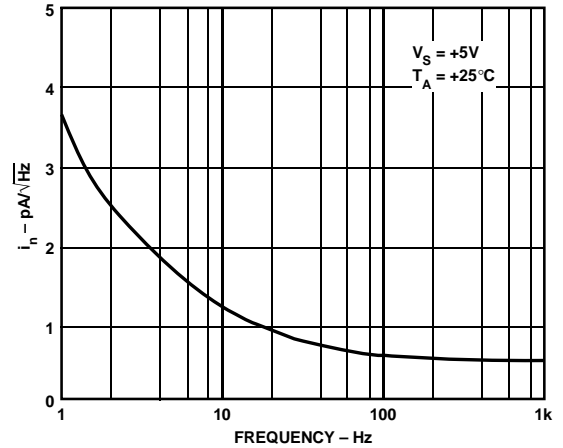


Figure 10. Current Noise Density vs. Frequency

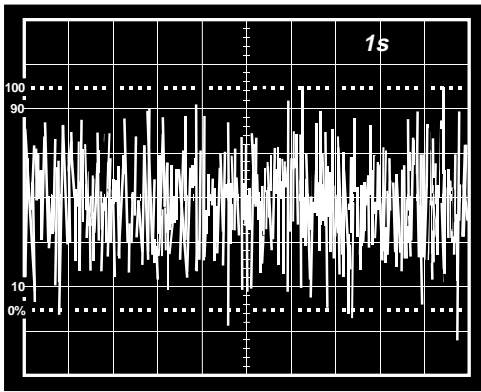


Figure 8. Input Voltage Noise (20 nV/div)

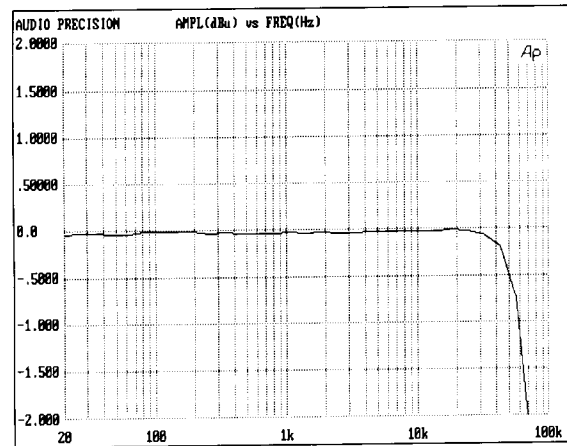


Figure 11. Frequency Response ($A_V = +1$, $V_S = +5\text{ V}$, $V_{IN} = 1\text{ V p-p}$, $R_L = 10\text{ k}\Omega$)

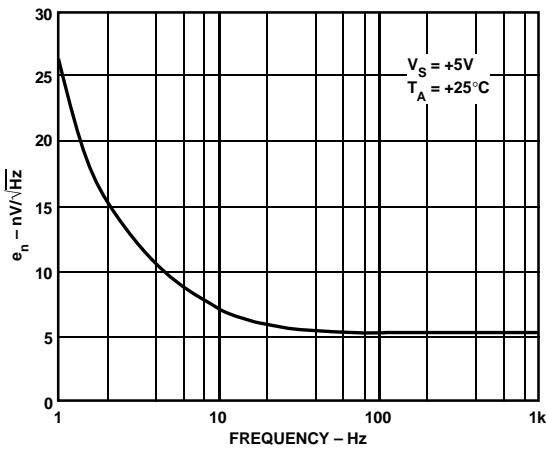


Figure 9. Voltage Noise Density vs. Frequency

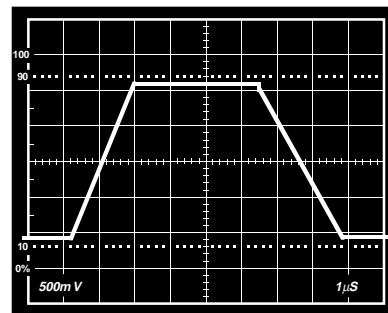


Figure 12. Square Wave Response ($V_S = +5\text{ V}$, $A_V = +1$, $R_L = \infty$)

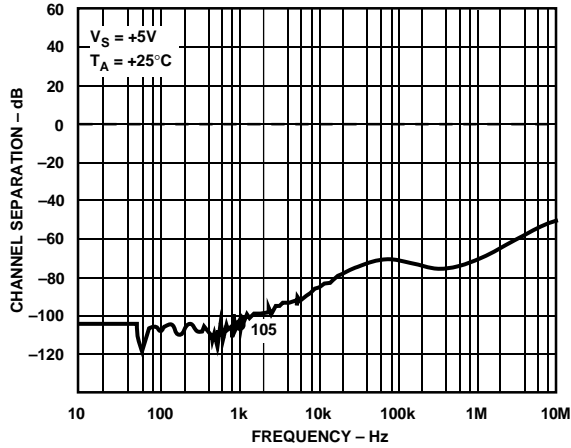


Figure 13. Crosstalk vs. Frequency ($R_L = 10\text{ k}\Omega$)

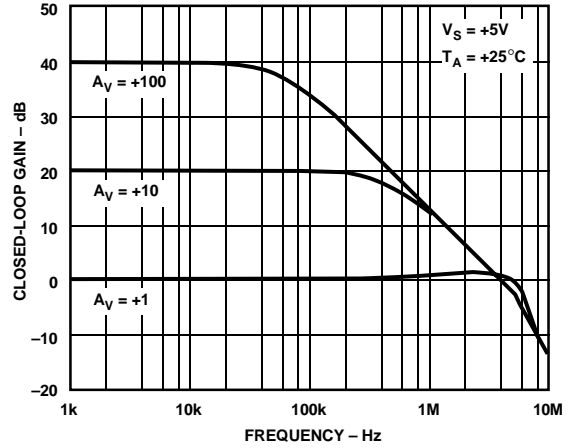


Figure 16. Closed-Loop Gain vs. Frequency

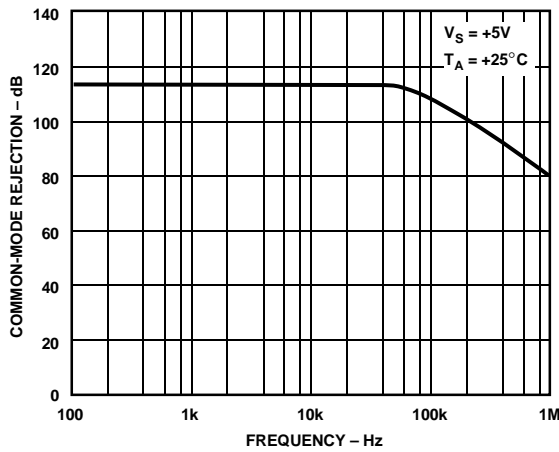


Figure 14. Common-Mode Rejection vs. Frequency

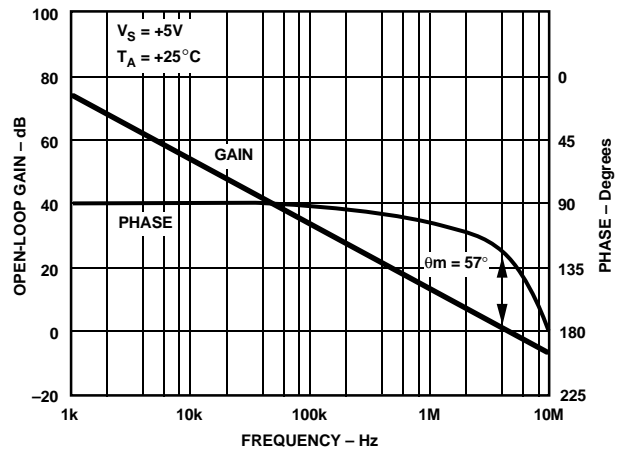


Figure 17. Open-Loop Gain and Phase vs. Frequency

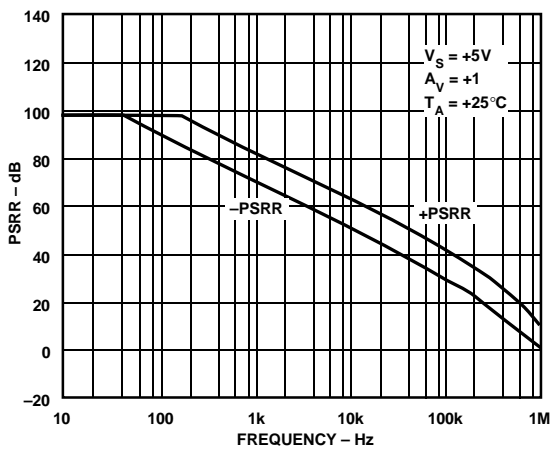


Figure 15. Power Supply Rejection vs. Frequency

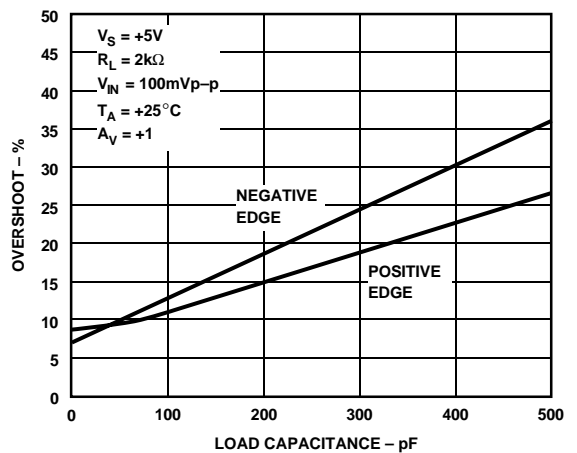


Figure 18. Small Signal Overshoot vs. Load Capacitance

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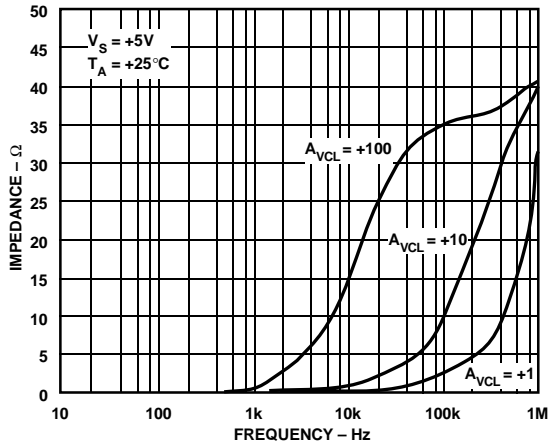


Figure 19. Output Impedance vs. Frequency

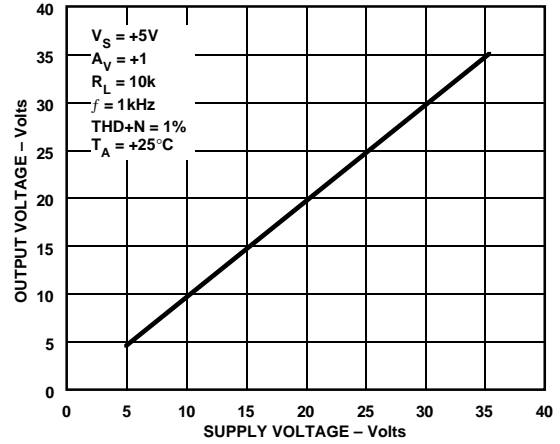


Figure 22. Output Swing vs. Supply Voltage

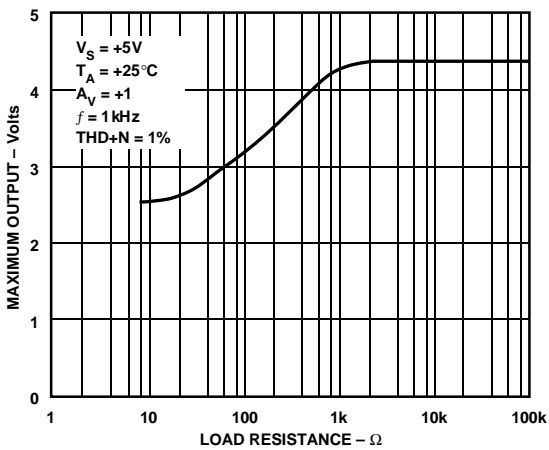


Figure 20. Maximum Output Voltage vs. Load Resistance

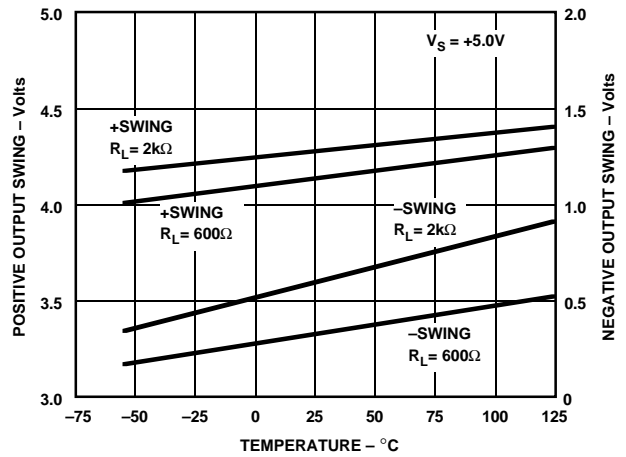


Figure 23. Output Swing vs. Temperature and Load

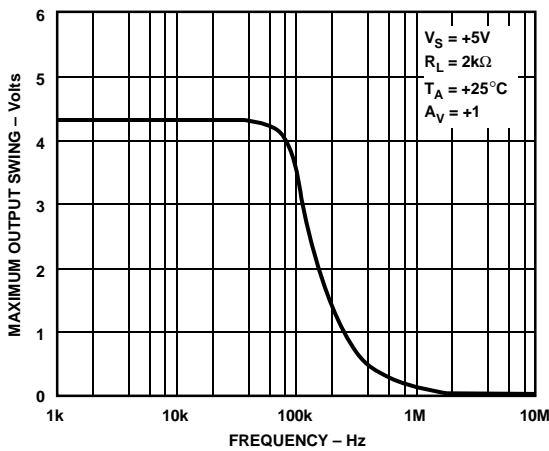


Figure 21. Maximum Output Swing vs. Frequency

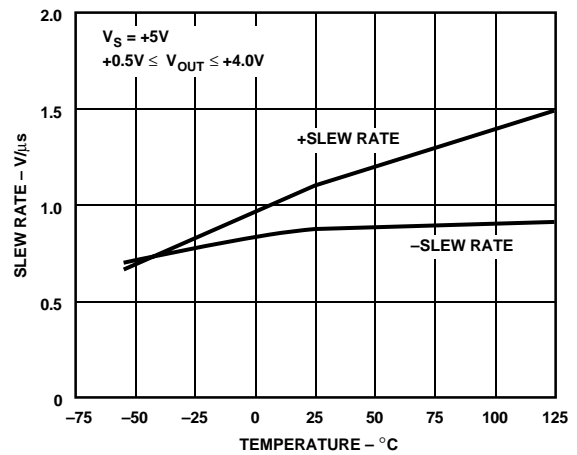


Figure 24. Slew Rate vs. Temperature

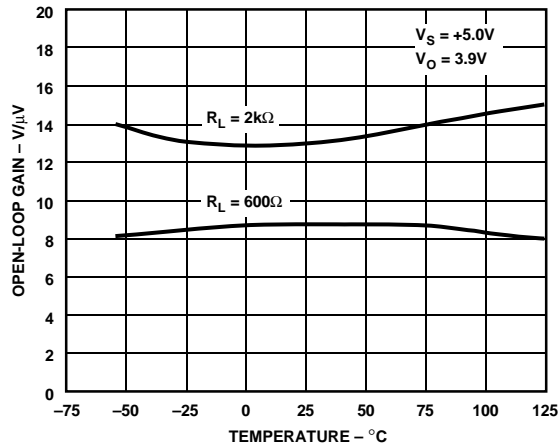


Figure 25. Open-Loop Gain vs. Temperature

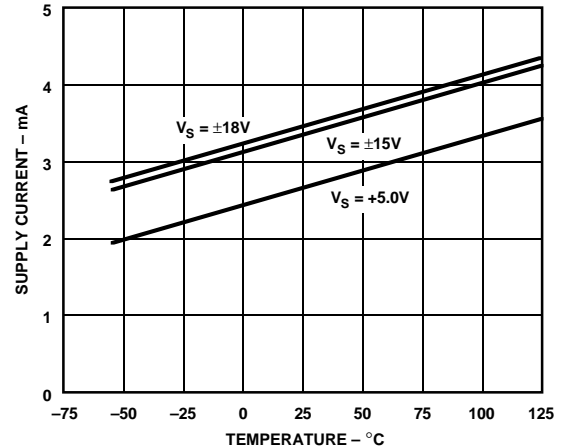


Figure 27. Supply Current vs. Temperature

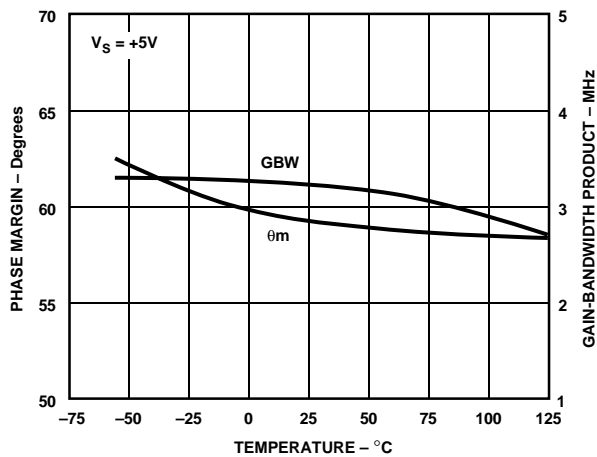


Figure 26. Gain Bandwidth Product and Phase Margin vs. Temperature

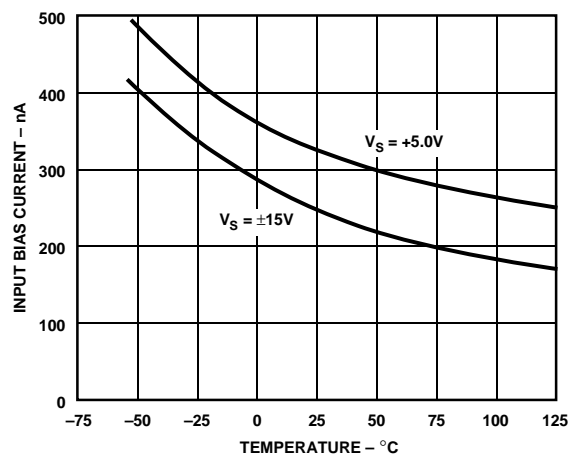


Figure 28. Input Bias Current vs. Temperature

APPLICATION INFORMATION

The SSM2135 is a low voltage audio amplifier that has exceptionally low noise and excellent sonic quality even when driving loads as small as 25 Ω . Designed for single supply use, the SSM2135's inputs common-mode and output swing to zero volts. Thus with a supply voltage at +5 V, both the input and output will swing from 0 V to +4 V. Because of this, signal dynamic range can be optimized if the amplifier is biased to a +2 V reference rather than at half the supply voltage.

The SSM2135 is unity-gain stable, even when driving into a fair amount of capacitive load. Driving up to 500 pF does not cause any instability in the amplifier. However, overshoot in the frequency response increases slightly.

The SSM2135 makes an excellent output amplifier for +5 V only audio systems such as a multimedia workstation, a CD output amplifier, or an audio mixing system. The amplifier has large output swing even at this supply voltage because it is designed to swing to the negative rail. In addition, it easily drives load impedances as low as 25 Ω with low distortion.

The SSM2135 is fully protected from phase reversal for inputs going to the negative supply rail. However, an internal ESD protection diodes will turn "on" when either input is forced more than 0.5 V below the negative rail. Under this condition, input current in excess of 2 mA may cause erratic output behavior, in which case a current limiting resistor should be included in the offending input if phase integrity is required with excessive input voltages. A 500 Ω or higher series input resistor will prevent phase inversion even with the input pulled 1 volt below the negative supply.

"Hot" plugging the input to a signal generally does not present a problem for the SSM2135, assuming the signal does not have any voltage exceeding the device's supply voltage. If so, it is advisable to add a series input resistor to limit the current, as well as a Zener diode to clamp the input to a voltage no higher than the supply.

SSM2135

APPLICATION CIRCUITS

A Low Noise Stereo Headphone Driver Amplifier

Figure 29 shows the SSM2135 used in a stereo headphone driver for multimedia applications with the AD1848, a 16-bit stereo codec. The SSM2135 is equally well suited for the serial-based AD1849 stereo codec. The headphone's impedance can be as low as 25 Ω, which covers most commercially available high fidelity headphones. Although the amplifier can operate at up to ±18 V supply, it is just as efficient powered by a single +5 V. At this voltage, the amplifier has sufficient output drive to deliver distortion-free sound to a low impedance headphone.

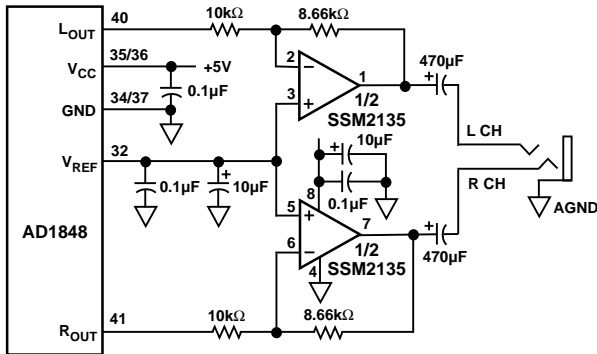


Figure 29. A Stereo Headphone Driver for Multimedia Sound Codec

Figure 30 shows the total harmonic distortion characteristics versus frequency driving into a 32 Ω load, which is a very typical impedance for a high quality stereo headphone. The SSM2135 has excellent power supply rejection, and as a result, is tolerant of poorly regulated supplies. However, for best sonic quality, the power supply should be well regulated and heavily bypassed to minimize supply modulation under heavy loads. A minimum of 10 μF bypass is recommended.

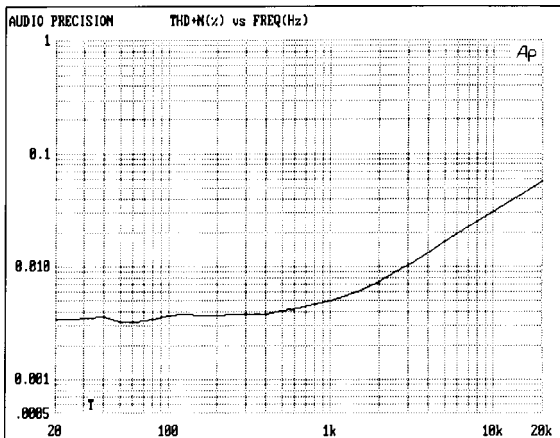


Figure 30. Headphone Driver THD+N vs. Frequency into a 32 Ω Load ($V_S = +5 V$, with 80 kHz Low-Pass Filter)

A Low Noise Microphone Preamplifier

The SSM2135's 4.7 nV/√Hz input noise in conjunction with low distortion makes it an ideal device for amplifying low level signals such as those produced by microphones. Figure 31 illustrates a stereo microphone input circuit feeding a multimedia sound codec. As shown, the gain is set at 100 (40 dB), although it can be set to other gains depending on the microphone output levels. Figure 32 shows the preamplifier's harmonic distortion performance with 1 V rms output while operating from a single +5 V supply.

The SSM2135 is biased to 2.25 V by the V_{REF} pin of the AD1848 codec. The same voltage is buffered by the 2N4124 transistor to provide "phantom power" to the microphone. A typical electret condenser microphone with an impedance range of 100 Ω to 1 kΩ works well with the circuit. This power booster circuit may be omitted for dynamic microphone elements.

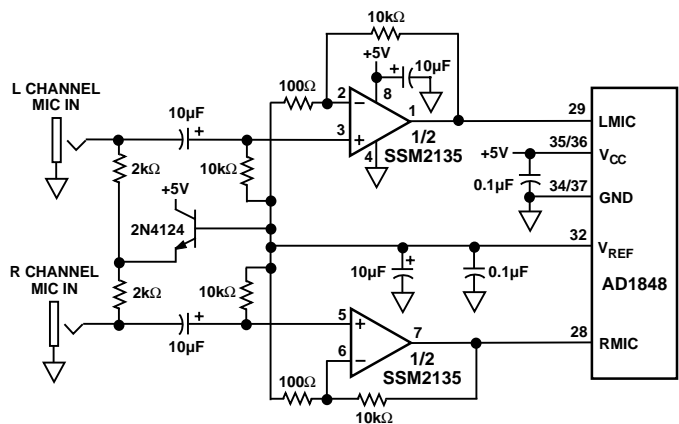


Figure 31. Low Noise Microphone Preamp for Multimedia Sound Codec

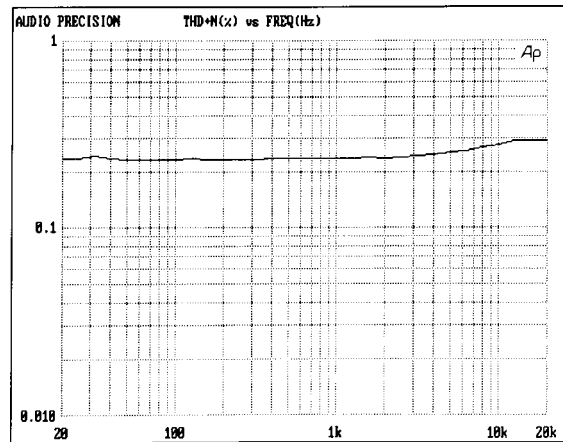


Figure 32. MIC Preamp THD+N Performance ($V_S = +5 V$, $A_V = 40 dB$, $V_{OUT} = 1 V rms$, with 80 kHz Low-Pass Filter)

An 18-Bit Stereo CD-DAC Output Amplifier

The SSM2135 makes an ideal single supply stereo output amplifier for audio D/A converters because of its low noise and distortion. Figure 33 shows the implementation of an 18-bit stereo DAC channel. The output amplifier also provides low-pass filtering for smoothing the oversampled audio signal. The filter's cutoff frequency is set at 22.5 kHz and it has a maximally flat response from dc to 20 kHz.

As mentioned above, the amplifier's outputs can drive directly into a stereo headphone that has impedance as low as 25 Ω with no additional buffering required.

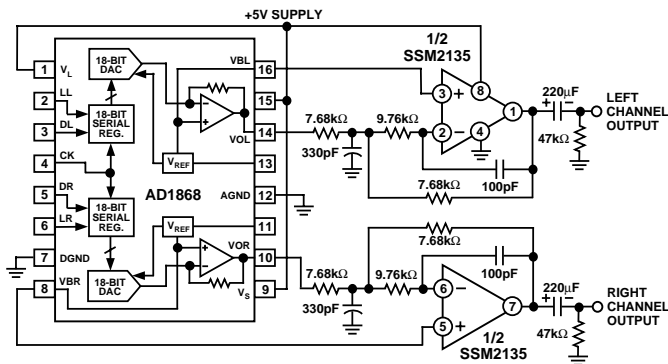


Figure 33. +5 V Stereo 18-Bit DAC

A Single Supply Differential Line Driver

Signal distribution and routing is often required in audio systems, particularly portable digital audio equipment for professional applications. Figure 34 shows a single supply line driver circuit that has differential output. The bottom amplifier provides a 2 V dc bias for the differential amplifier in order to maximize the output swing range. The amplifier can output a maximum of 0.8 V rms signal with a +5 V supply. It is capable of driving into 600 Ω line termination at a reduced output amplitude.

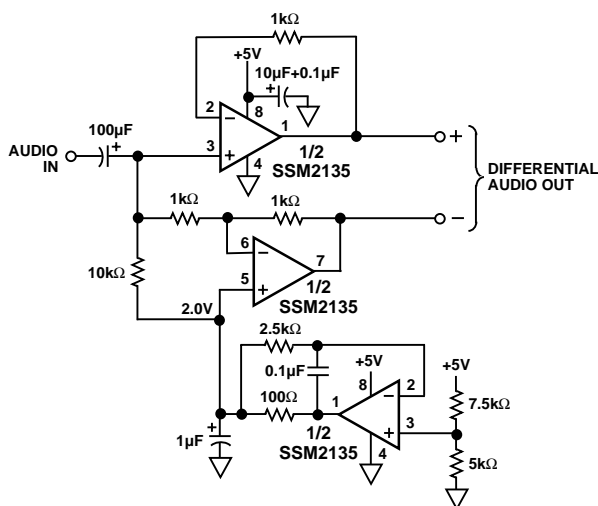


Figure 34. Single Supply Differential Line Driver

A Single Supply Differential Line Receiver

Receiving a differential signal with minimum distortion is achieved using the circuit in Figure 35. Unlike a difference amplifier (a subtractor), the circuit has a true balanced input impedance regardless of input drive levels. That is, each input always presents a 20 k Ω impedance to the source. For best common-mode rejection performance, all resistors around the differential amplifier must be very well matched. Best results can be achieved using a 10 k Ω precision resistor network.

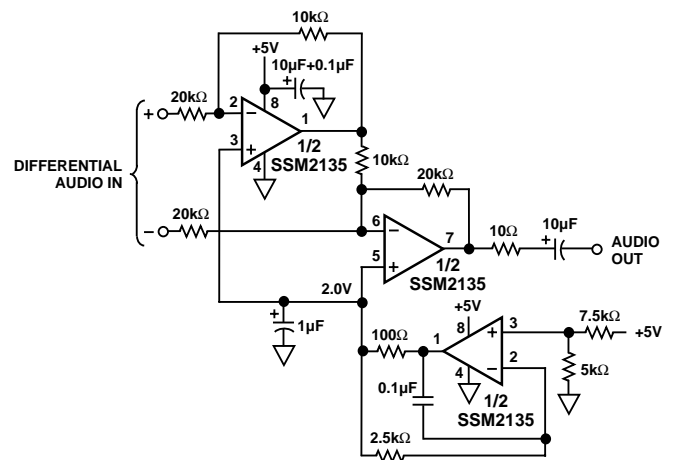


Figure 35. Single Supply Balanced Differential Line Receiver

A Pseudo-Reference Voltage Generator

For single supply circuits, a reference voltage source is often required for biasing purposes or signal offsetting purposes. The circuit in Figure 36 provides a supply splitter function with low output impedance. The 1 μ F output capacitor serves as a charge reservoir to handle a sudden surge in demand by the load as well as providing a low ac impedance to it. The 0.1 μ F feedback capacitor compensates the amplifier in the presence of a heavy capacitive load, maintaining stability.

The output can source or sink up to 12 mA of current with +5 V supply, limited only by the 100 Ω output resistor. Reducing the resistance will increase the output current capability. Alternatively, increasing the supply voltage to 12 V also improves the output drive to more than 25 mA.

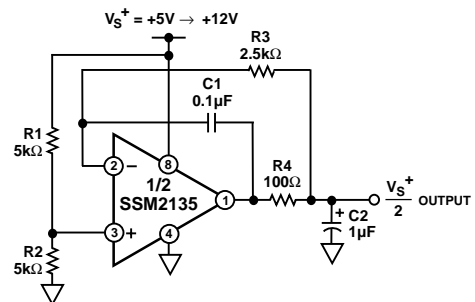


Figure 36. Pseudo-Reference Generator

SSM2135

A Digital Volume Control Circuit

Working in conjunction with the AD7528/PM7528 dual 8-bit D/A converter, the SSM2135 makes for an efficient audio attenuator, as shown in Figure 37. The circuit works off a single +5 V supply. The DAC's are biased to a 2 V reference level which is sufficient to keep the DAC's internal R-2R ladder switches operating properly. This voltage is also the optimal midpoint of the SSM2135's common-mode and output swing range. With the circuit as shown, the maximum input and output swing is 1.25 V rms. Total harmonic distortion measures a respectable 0.01% at 1 kHz and 0.1% at 20 kHz. The frequency response at any attenuation level is flat to 20 kHz.

Each DAC can be controlled independently via the 8-bit parallel data bus. The attenuation level is linearly controlled by the binary weighting of the digital data input. Total attenuation ranges from 0 dB to 48 dB.

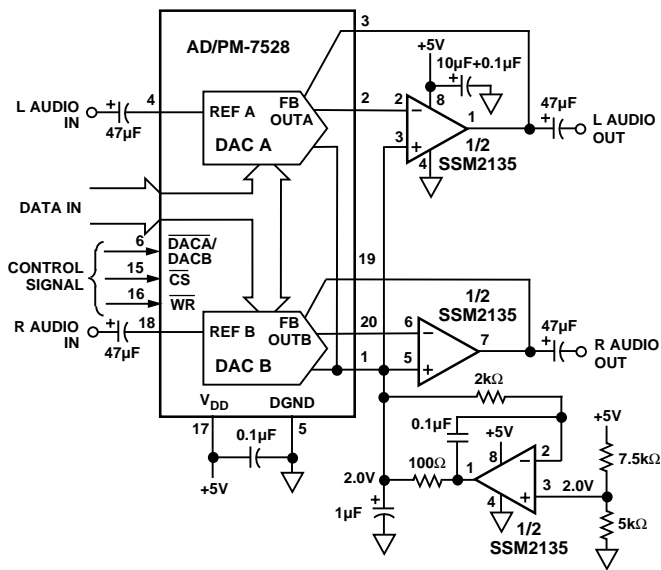


Figure 37. Digital Volume Control

A Logarithmic Volume Control Circuit

Figure 38 shows a logarithmic version of the volume control function. Similar biasing is used. With an 8-bit bus, the AD7111 provides an 88.5 dB attenuation range. Each bit resolves a 0.375 dB attenuation. Refer to AD7111 data sheet for attenuation levels for each input code.

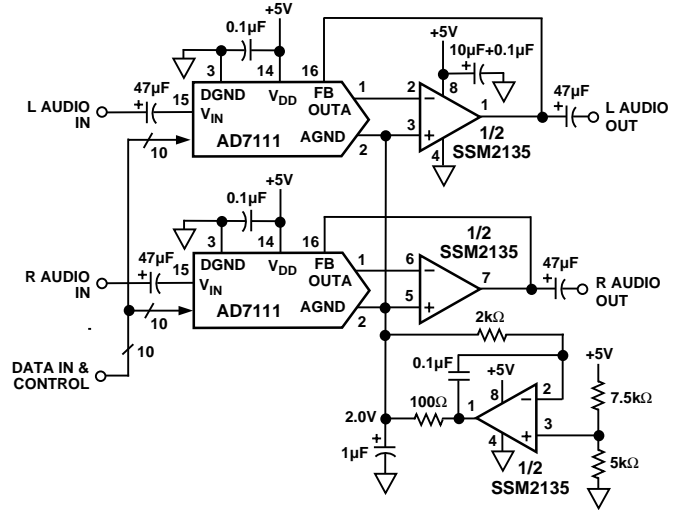


Figure 38. Single Supply Logarithmic Volume Control

SPICE MACROMODEL

*SSM2135 SPICE Macro-Model 9/92, Rev. A

* JCB/ADI

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*Node Assignments

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|--|--------------------|---|-----------------|---|-----------------|--|-----------------|--|--------|
| | Noninverting Input | | Inverting Input | | Positive Supply | | Negative Supply | | Output |
| | | | | | | | | | |
| | 3 | 2 | 7 | 4 | 6 | | | | |

.SUBCKT SSM2135

*

* INPUT STAGE

R3 4 19 1.5E3

R4 4 20 1.5E3

C1 19 20 5.311E-12

I1 7 18 106E-6

IOS 2 3 25E-09

EOS 12 5 POLY(1) 51 4 25E-06 1

Q1 19 3 18 PNP1

Q2 20 12 18 PNP1

CIN 3 2 3E-12

D1 3 1 DY

D2 2 1 DY

EN 5 2 22 0 1

GN1 0 2 25 0 1E-5

GN2 0 3 28 0 1E-5

*

* VOLTAGE NOISE SOURCE WITH FLICKER NOISE

DN1 21 22 DEN

DN2 22 23 DEN

VN1 21 0 DC 2

VN2 0 23 DC 2

*

* CURRENT NOISE SOURCE WITH FLICKER NOISE

DN3 24 25 DIN

DN4 25 26 DIN

VN3 24 0 DC 2

VN4 0 26 DC 2

*

* SECOND CURRENT NOISE SOURCE

DN5 27 28 DIN

DN6 28 29 DIN

VN5 27 0 DC 2

VN6 0 29 DC 2

*

* GAIN STAGE & DOMINANT POLE AT .2000E+01 HZ

G2 34 36 19 20 2.65E-04

R7 34 36 39E+06

V3 35 4 DC 6

D4 36 35 DX

VB2 34 4 1.6

*

* SUPPLY/2 GENERATOR

ISY 7 4 0.2E-3

R10 7 60 40E+3

R11 60 4 40E+3

C3 60 0 1E-9

*

* CMRR STAGE & POLE AT 6 kHz

ECM 50 4 POLY(2) 3 60 2 60 0 1.6 1.6

CCM 50 51 26.5E-12

RCM1 50 51 1E6

RCM2 51 4 1

*

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OUTPUT STAGE

R12 37 36 1E3

R13 38 36 500

C4 37 6 20E-12

C5 38 39 20E-12

M1 39 36 4 4 MN L=9E-6 W=1000E-6 AD=15E-9 AS=15E-9

M2 45 36 4 4 MN L=9E-6 W=1000E-6 AD=15E-9 AS=15E-9

5 39 47 DX

D6 47 45 DX

Q3 39 40 41 QPA 8

VB 7 40 DC 0.861

R14 7 41 375

Q4 41 7 43 QNA 1

R17 7 43 15

Q5 43 39 6 QNA 20

Q6 46 45 6 QPA 20

R18 46 4 15

Q7 36 46 4 QNA 1

M3 6 36 4 4 MN L=9E-6 W=2000E-6 AD=30E-9 AS=30E-9

*

* NONLINEAR MODELS USED

*

.MODEL DX D (IS=1E-15)

.MODEL DY D (IS=1E-15 BV=7)

.MODEL PNP1 PNP (BF=220)

.MODEL DEN D (IS=1E-12 RS=1016 KF=3.278E-15 AF=1)

.MODEL DIN D (IS=1E-12 RS=100019 KF=4.173E-15 AF=1)

.MODEL QNA NPN (IS=1.19E-16 BF=253 VAF=193 VAR=15 RB=2.0E3

+ IRB=7.73E-6 RBM=132.8 RE=4 RC=209 CJE=2.1E-13 VJE=0.573

+ MJE=0.364 CJC=1.64E-13 VJC=0.534 MJC=0.5 CJS=1.37E-12

+ VJS=0.59 MJS=0.5 TF=0.43E-9 PTF=30)

.MODEL QPA PNP (IS=5.21E-17 BF=131 VAF=62 VAR=15 RB=1.52E3

+ IRB=1.67E 5-RBM=368.5 RE=6.31 RC=354.4 CJE=1.1E-13

+ VJE=0.745 MJE=0.33 CJC=2.37E-13 VJC=0.762 MJC=0.4

+ CJS=7.11E-13 VJS=0.45 MJS=0.412 TF=1.0E-9 PTF=30)

.MODEL MN NMOS (LEVEL=3 VTO=1.3 RS=0.3 RD=0.3 TOX=8.5E-8

+ LD=1.48E-6 WDW=1E-6 NSUB=1.53E16 UO=650 DELTA= 10VMAX=2E5

+ XJ=1.75E-6 KAPPA=0.8 ETA=0.066 THETA=0.01 TPG=1 CJ=2.9E-4

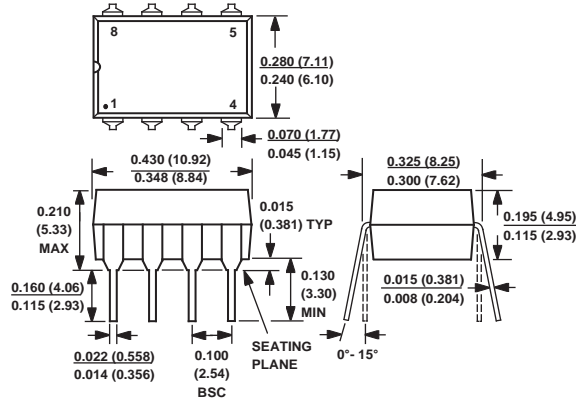
+ PB=0.837 MJ=0.407 CJSW=0.5E-9 MJSW=0.33)

*

.ENDS SSM-2135

OUTLINE DIMENSIONS
 Dimensions shown in inches and (mm).

8-Lead Plastic DIP (N-8)



8-Lead Narrow-Body (SO-8)

