

## N-Channel Enhancement-Mode Vertical DMOS FETs

#### **Ordering Information**

BV <sub>DSS</sub> /	R <sub>DS(ON)</sub>	Order Number / Package				
BV <sub>DGS</sub>	(max)	TO-92	TO-236AB*	Die <sup>†</sup>		
60V	4.0Ω	VN2106N3	_	_		
100V	4.0Ω	_	VN2110K1	VN2110ND		

<sup>†</sup>MIL visual screening available

\*Same as SOT-23. All units shipped on 3,000 piece carrier tape reels.

#### Features

- Commercial and Military versions available
- □ Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- □ Low C<sub>ISS</sub> and fast switching speeds
- □ High input impedance and high gain

# Applications

- Motor controls
- Amplifiers
- Power supply circuits
- Converters
- Switches
- Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

# **Absolute Maximum Ratings**

Drain-to-Source Voltage	BV <sub>DSS</sub>
Drain-to-Gate Voltage	BV <sub>DGS</sub>
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

\* Distance of 1.6 mm from case for 10 seconds.

#### 11/12/01

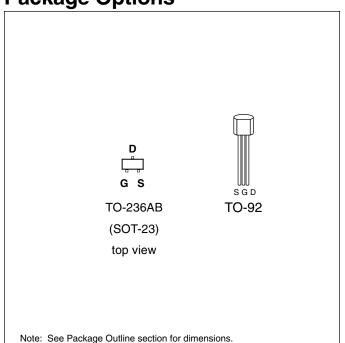
Product marking for SOT-23:					
	N1A*				
where $* = 2$ -week alpha date code					

## Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

#### **Package Options**



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# **Thermal Characteristics**

Package	I <sub>D</sub> (continuous)⁺	I <sub>D</sub> (pulsed)	Power Dissipation* @ T <sub>C</sub> = 25°C	θ <sub>jc</sub> °C/W	θ <sub>ja</sub> °C/W	I <sub>DR</sub> †	I <sub>DRM</sub>
TO-92	0.3A	1.0A	1.0W	125	170	0.3A	1.0A
TO-236AB	0.2A	0.8A	0.36W (T <sub>A</sub> = 25°C)	200	350	0.2A	0.8A

 $^{\dagger}I_{D}$  (continuous) is limited by max rated  $T_{j}$ .

\* Total for package.

# Electrical Characteristics (@ 25°C unless otherwise specified)

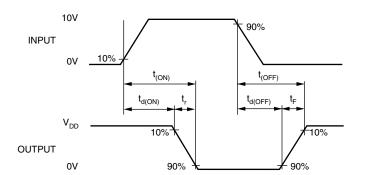
Symbol	Parameter		Min	Тур	Max	Unit	Conditions	
$BV_{DSS}$	Drain-to-Source	VN2110	100			v	$I_{D} = 1 \text{mA}, V_{GS} = 0 \text{V}$	
200	Breakdown Voltage	VN2106	60					
V <sub>GS(th)</sub>	Gate Threshold Voltage		0.8		2.4	V	$V_{GS} = V_{DS}, I_D = 1mA$	
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-3.8	-5.5	mV/°C	$V_{GS} = V_{DS}, I_{D} = 1mA$	
I <sub>GSS</sub>	Gate Body Leakage			0.1	100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$	
I <sub>DSS</sub>	Zero Gate Voltage Drain Curr				1	μA	$V_{GS} = 0V, V_{DS} = Max Rating$	
					100	μΑ	$V_{GS} = 0V, V_{DS} = 0.8 \text{ Max Rating}$ $T_A = 125^{\circ}\text{C}$	
I <sub>D(ON)</sub>	ON-State Drain Current		0.6			А	$V_{GS} = 10V, V_{DS} = 25V$	
R <sub>DS(ON)</sub>	Static Drain-to-Source			4.5	6.0	Ω	$V_{GS} = 5V, I_{D} = 75mA$	
	ON-State Resistance			3.0	4.0	Ω	$V_{GS} = 10V, I_{D} = 500mA$	
$\Delta R_{DS(ON)}$	Change in R <sub>DS(ON)</sub> with Temperature			0.70	1.0	%/°C	$V_{GS} = 10V, I_{D} = 500mA$	
G <sub>FS</sub>	Forward Transconductance		150	400		mប	$V_{DS} = 25V, I_{D} = 0.5A$	
C <sub>ISS</sub>	Input Capacitance			35	50			
C <sub>OSS</sub>	Common Source Output Capacitance			13	25	pF	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 25V, f = 1MH:	
C <sub>RSS</sub>	Reverse Transfer Capacitanc	e		4	5			
t <sub>d(ON)</sub>	Turn-ON Delay Time Rise Time			3	5	ns	$V_{DD} = 25V$ $I_D = 0.6A$	
t <sub>r</sub>				5	8			
t <sub>d(OFF)</sub>	Turn-OFF Delay Time			6	9		$R_{GEN} = 25\Omega$	
t <sub>f</sub>	Fall Time			5	8			
V <sub>SD</sub>	Diode Forward Voltage Drop			1.2	1.8	V	$I_{SD} = 0.6A, V_{GS} = 0V$	
t <sub>rr</sub>	Reverse Recovery Time			400		ns	I <sub>SD</sub> = 0.6A, V <sub>GS</sub> = 0V	

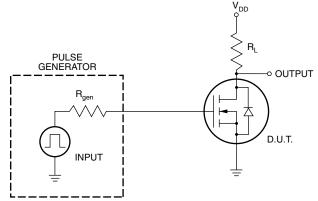
Notes:

1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)

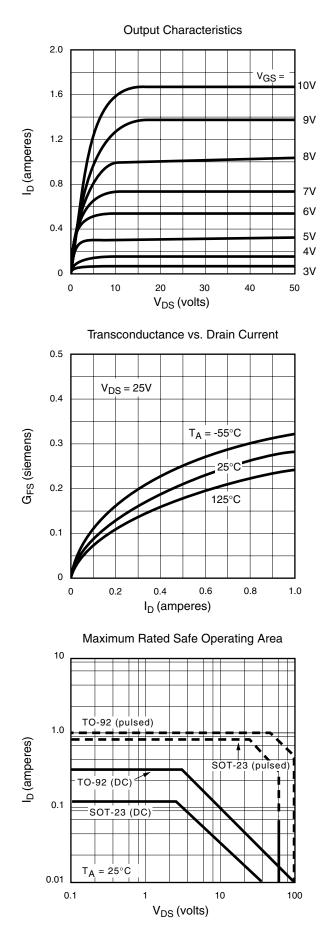
2. All A.C. parameters sample tested.

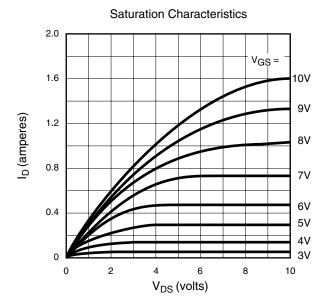




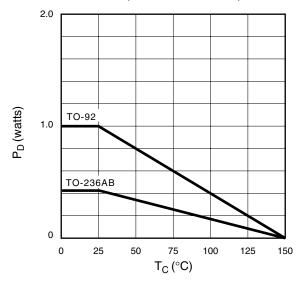


## **Typical Performance Curves**

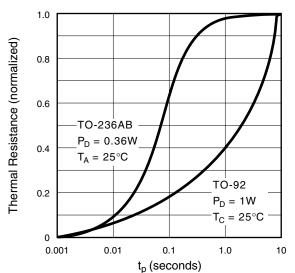




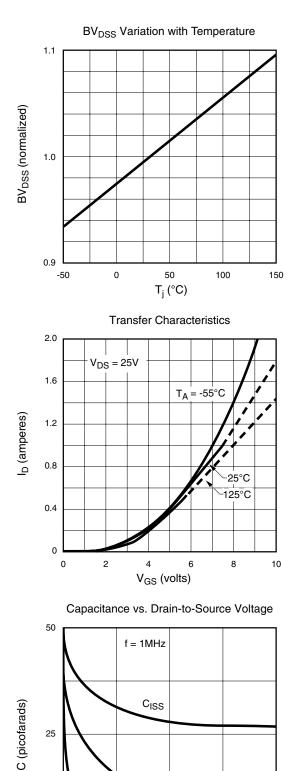
Power Dissipation vs. Case Temperature



Thermal Response Characteristics



### **Typical Performance Curves**

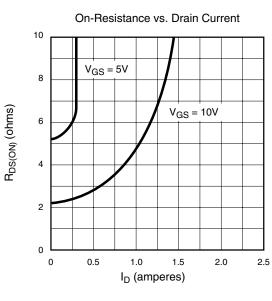




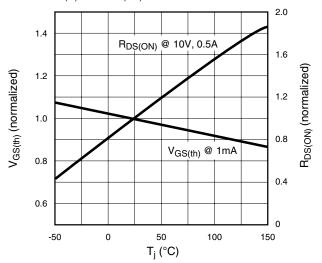
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0

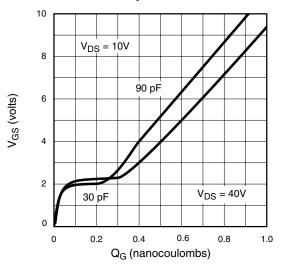
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 $V_{GS(th)}$  and  $R_{DS(ON)}$  Variation with Temperature



Gate Drive Dynamic Characteristics



11/12/01

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C<sub>OSS</sub>

C<sub>RSS</sub>

20

V<sub>DS</sub> (volts)

40

30

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