DATA SHEET

P82B96
Dual bi-directional bus buffer

Product data
Supersedes data of 2003 Feb 20

2003 Apr 02

Philips
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Dual bi-directional bus buffer P82B96

FEATURES

- Dual Interface handles both SCL and SDA I^2C signals
- Bi-directional data transfer
- Splits I^2C signal into forward/reverse Tx, Ty, Rx and Ry signals
- Low power supply current
- Wide supply voltage range (I^2C logic levels at Sx Sy independent of IC supply voltage)
- Supply voltage range of 2 V to 15 V
- 60 mA sink capability for driving low impedance buses
- Clock speeds to 400 kHz on short buses or where delays permit
- ESD protection exceeds 3500 V HBM per JESD22-A114 and 1000 V CDM per JESD22-C101
- Latch-up free (bipolar process with no latching structures)

TYPICAL APPLICATIONS

- Interface between I^2C buses operating at different logic levels (e.g., 5 V and 3 V or 15 V)
- Interface between I^2C and SMB (350 μA) bus standard.
- Simple conversion of I^2C SDA or SCL signals to multi-drop differential bus hardware, e.g., via compatible PCA82C250.
- Interfaces with Opto-couplers to provide Opto isolation between I^2C bus nodes.

DESCRIPTION

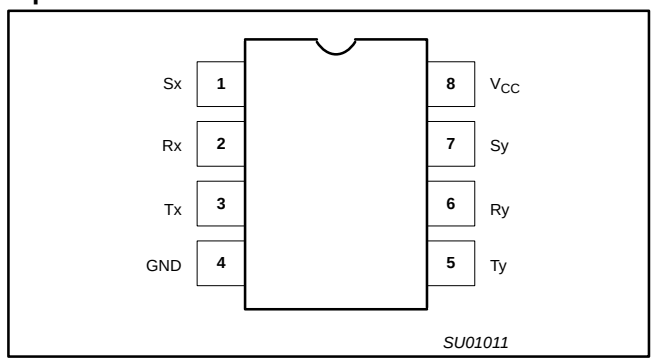
The P82B96 is a bipolar IC that creates a non-latching, bi-directional, logic interface between the normal I^2C bus and a range of other bus configurations. It can interface I^2C bus logic signals to similar buses having different voltage and current levels.

For example it can interface to the 350 μA SMB bus, to 3.3 V logic devices, and to 15 V levels and/or low impedance lines to improve noise immunity on longer bus lengths.

It achieves this interface without any restrictions on the normal I^2C protocols or clock speed. The IC adds minimal loading to the I^2C node, and loadings of the new bus or remote I^2C nodes are not transmitted or transformed to the local node. Restrictions on the number of I^2C devices in a system, or the physical separation between them, are virtually eliminated. Transmitting SDA/SCL signals via balanced transmission lines (twisted pairs) or with galvanic isolation (opto-coupling) is simple because separate directional Tx and Rx signals are provided. The Tx and Rx signals may be directly connected, without causing latching, to provide an alternative bi-directional signal line with I^2C properties.

PIN CONFIGURATIONS

8-pin dual in-line or SO



PINNING

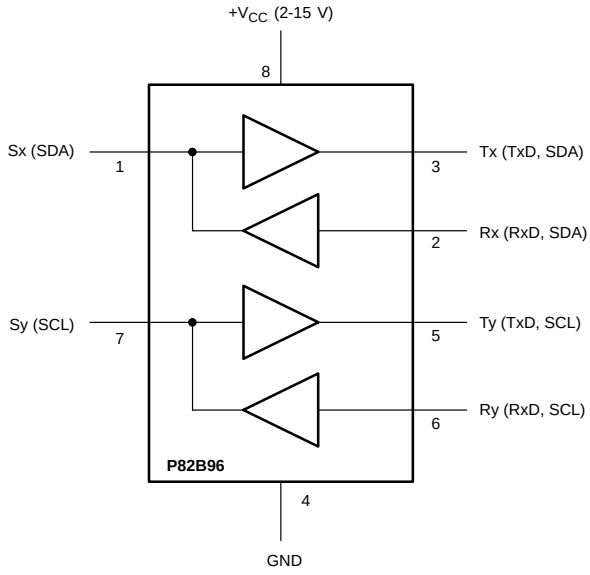
SYMBOL	PIN	DESCRIPTION
Sx	1	I^2C Bus (SDA or SCL)
Rx	2	Receive signal
Tx	3	Transmit signal
GND	4	Negative Supply
Ty	5	Transmit signal
Ry	6	Receive signal
Sy	7	I^2C Bus (SDA or SCL)
V_{CC}	8	Positive supply

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	TOPSIDE MARK	DRAWING NUMBER
8-pin plastic dual In-line package	-40 to +85 °C	P82B96PN	P82B96PN	SOT97-1
8-pin plastic small outline package	-40 to +85 °C	P82B96TD	P82B96T	SOT96-1

NOTES:
1. Standard packing quantities and other packaging data are available at www.philipslogic.com/packaging.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The P82B96 has two identical buffers allowing buffering of both of the I^2C (SDA and SCL) signals. Each buffer is made up of two logic signal paths, a forward path from the I^2C interface pin which drives the buffered bus, and a reverse signal path from the buffered bus input to drive the I^2C bus interface.

Thus these paths are:

1. Sense the voltage state of the I^2C pin Sx (or Sy) and transmit this state to the pin Tx (Ty resp.), and
2. Sense the state of the pin Rx (Ry) and pull the I^2C pin low whenever Rx (Ry) is low.

The rest of this discussion will address only the “x” side of the buffer: the “y” side is identical.

The I^2C pin (Sx) is designed to interface with a normal I^2C bus.

The logic threshold voltage levels on the I^2C bus are independent of the IC supply V_{CC} The maximum I^2C bus supply voltage is 15 V and the guaranteed static sink current is 3 mA.

The logic level of Rx is determined from the power supply voltage V_{CC} of the chip. Logic LOW is below 42 % of V_{CC} and logic HIGH is above 58 % of V_{CC}: with a typical switching threshold of half V_{CC}.

Tx is an open collector output without ESD protection diodes to V_{CC}. It may be connected via a pull-up resistor to a supply voltage in excess of $V_{CC,}$ as long as the 15 V rating is not exceeded. It has a larger current sinking capability than a normal I^2C device, being able to sink a static current of greater than 30 mA, and typical 100 mA dynamic pull-down capability as well.

A logic LOW is only transmitted to Tx when the voltage at the I^2C pin (Sx) is below 0.6 V. A logic LOW at Rx will cause the I^2C bus (Sx) to be pulled to a logic LOW level in accordance with I^2C requirements (max. 1.5 V in 5 V applications) but not low enough to be looped back to the Tx output and cause the buffer to latch low.

The minimum LOW level this chip can achieve on the I^2C bus by a LOW at Rx is typically 0.8 V.

If the supply voltage V_{cc} fails then neither the I^2C nor the Tx output will be held low. Their open collector configuration allows them to be pulled up to the rated maximum of 15 V even without V_{CC} present. The input configuration on Sx and Rx also present no loading of external signals even when V_{CC} is not present.

The effective input capacitance of any signal pin, measured by its effect on bus rise times, is less than 7 pF for all bus voltages and supply voltages including V_{CC} = 0 V.

MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages with respect to pin GND (pin 4).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC} to GND	Supply voltage range V_{CC}	-0.3	+18	V
V_{bus}	Voltage range on I^2C Bus, SDA or SCL	-0.3	+18	V
V_{Tx}	Voltage range on buffered output	-0.3	+18	V
V_{Rx}	Voltage range on receive input	-0.3	+18	V
I	DC current (any pin)	—	250	mA
R_{tot}	Power dissipation	—	300	mW
T_{stg}	Storage temperature range	-55	+125	°C
T_{amb}	Operating ambient temperature range	-40	+85	°C

CHARACTERISTICS

At T_{amb} = 25 °C; Voltages are specified with respect to GND with V_{CC} = 5 V unless otherwise stated.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Power Supply					
V_{CC}	Supply voltage (operating)	2.0	—	15	V
I_{CC}	Supply current, buses HIGH	—	0.9	1.8	mA
I_{CC}	Supply current at V_{CC} = 15V, buses HIGH	—	1.1	2.5	mA
I_{CC}	Additional supply current per Tx or Ty LOW	—	1.7	3.5	mA
Bus pull-up (load) voltages and currents					
V_{Sx}, V_{Sy}	Maximum input/output voltage level Open collector I^2C bus and V_{Rx}, V_{Ry} = HIGH	—	—	15	V
I_{Sx}, I_{Sy}	Static output loading on I^2C bus V_{Sx}, V_{Sy} = 1.2 V V_{Rx}, V_{Ry} = LOW	0.2	—	3	mA
I_{Sx}, I_{Sy}	Dynamic output sink capability on I^2C bus V_{Sx}, V_{Sy} > 2 V V_{Rx}, V_{Ry} = LOW	7	18	—	mA
I_{Sx}, I_{Sy}	Leakage current on I^2C bus V_{Sx}, V_{Sy} = 5 V, and V_{Rx}, V_{Ry} = HIGH	—	—	1	μA
I_{Sx}, I_{Sy}	Leakage current on I^2C bus V_{Sx}, V_{Sy} = 15 V, and V_{Rx}, V_{Ry} = HIGH	—	1	—	μA
V_{Tx}, V_{Ty}	Maximum output voltage level Open collector	—	—	15	V
I_{Tx}, I_{Ty}	Static output loading on buffered bus V_{Tx}, V_{Ty} = 0.4 V V_{Sx}, V_{Sy} = LOW on I^2C bus = 0.4V	—	—	30	mA
I_{Tx}, I_{Ty}	Dynamic output sink capability, buffered bus: V_{Tx}, V_{Ty} > 1 V V_{Sx}, V_{Sy} = LOW on I^2C bus = 0.4V	60	100	—	mA
I_{Tx}, I_{Ty}	Leakage current on buffered bus V_{Tx}, V_{Ty} = V_{CC} = 15 V, and V_{Sx}, V_{Sy} = HIGH	—	1	—	μA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Input Currents					
I_{Sx}, I_{Sy}	Input current from I^2C bus, bus LOW V_{Rx}, V_{Ry} = HIGH	—	-1	—	μA
I_{Rx}, I_{Ry}	Input current from buffered bus, bus LOW V_{Rx}, V_{Ry} = 0.4 V	—	-1	—	μA
I_{Rx}, I_{Ry}	Leakage current on buffered bus input V_{Rx}, V_{Ry} = V_{CC}	—	1	—	μA
Input Thresholds					
V_{Sx}, V_{Sy}	Output logic level LOW, on normal I^2C bus I_{Sx}, I_{Sy} = 3 mA	0.8	0.9	1.0	V
V_{Sx}, V_{Sy}	Output logic level LOW, on normal I^2C bus I_{Sx}, I_{Sy} = 0.2 mA	—	750	—	mV
V_{Sx}, V_{Sy}	Input logic level LOW threshold On normal I^2C bus	600	650	—	mV
dV_{Sx}/dT, dV_{Sy}/dT	Temperature coefficient of thresholds	—	-2	—	mV/K
V_{Rx}, V_{Ry}	Input logic HIGH level Fraction of applied V_{CC}	0.58	—	—	
V_{Rx}, V_{Ry}	Input threshold Fraction of applied V_{CC}	—	0.5	—	
V_{Rx}, V_{Ry}	Input logic LOW level Fraction of applied V_{CC}	—	—	0.42	
Bus Release on V_{CC} Failure					
V_{Sx}, V_{Sy}, V_{Tx}, V_{Ty}	V_{CC} voltage at which all buses are guaranteed to be released	—	—	1	V
dV/dT	Temperature coefficient of guaranteed release voltage	—	-4	—	mV/K
Buffer response time					
$T_{fall\ delay}$ V_{Sx} to V_{Tx} V_{Sy} to V_{Ty}	Buffer time delay on FALLING input between V_{Sx} = input switching threshold: and V_{Tx} output falling 50%. R_{Tx} pull up = 160 Ω, no capacitive load, V_{CC} = 5 V	—	100	—	ns
$T_{rise\ delay}$ V_{Sx} to V_{Tx} V_{Sy} to V_{Ty}	Buffer time delay on RISING input between V_{Sx} = input switching threshold, and V_{Tx} output reaching 50%. R_{Tx} pull up = 160 Ω, no capacitive load, V_{CC} = 5 V	—	100	—	ns
$T_{fall\ delay}$ V_{Rx} to V_{Sx} V_{Ry} to V_{Sy}	Buffer time delay on FALLING input between V_{Rx} = input switching threshold, and V_{Sx} output falling 50%. R_{Sx} pull up = 1600 Ω, no capacitive load, V_{CC} = 5 V	—	300	—	ns
$T_{rise\ delay}$ V_{Rx} to V_{Sx} V_{Ry} to V_{Sy}	Buffer time delay on RISING input between V_{Rx} = input switching threshold, and V_{Sx} output reaching 50%. R_{Sx} pull up = 1600 Ω, no capacitive load, V_{CC} = 5 V	—	300	—	ns
Input capacitance					
Cin	Effective input capacitance of any signal pin measured by incremental bus rise times	—	—	7	pF

TYPICAL APPLICATIONS

See AN460 and AN255 for more application detail.

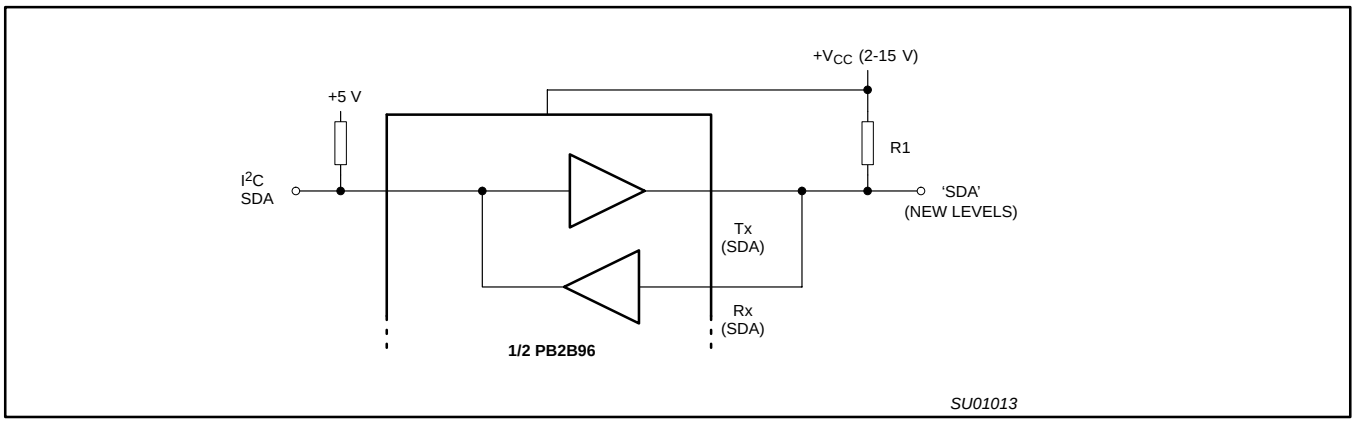


Figure 1. Interfacing an 'I^{2}C' type of bus with different logic levels.

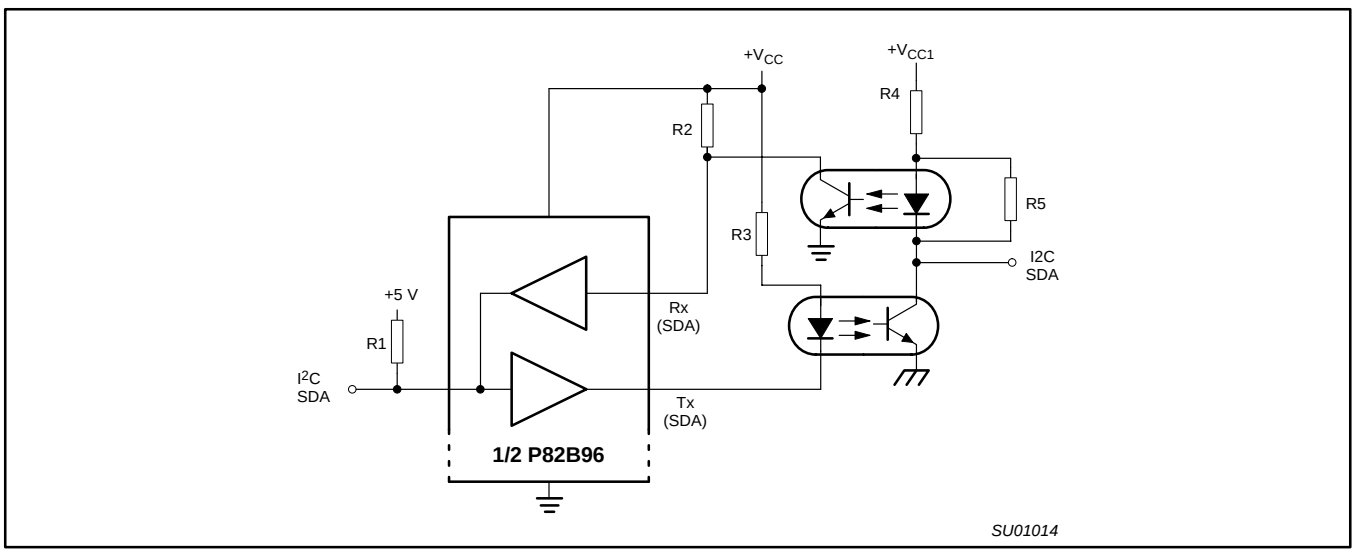


Figure 2. Galvanic isolation of I^{2}C nodes via opto-couplers

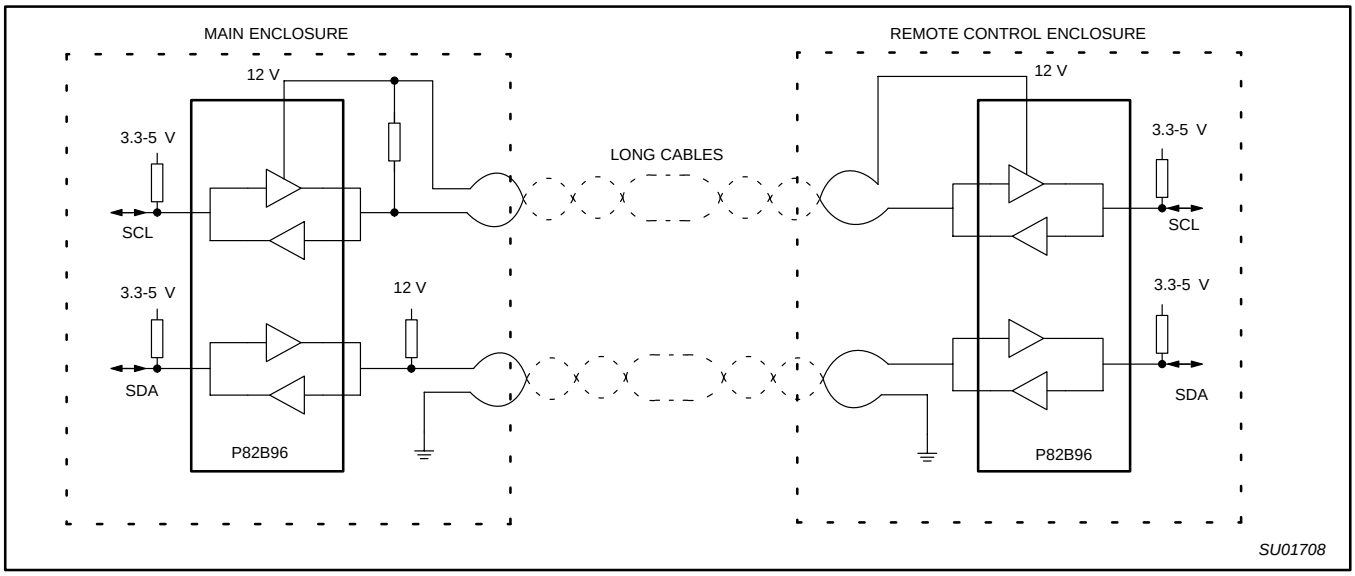


Figure 3. Long distance I²C communications

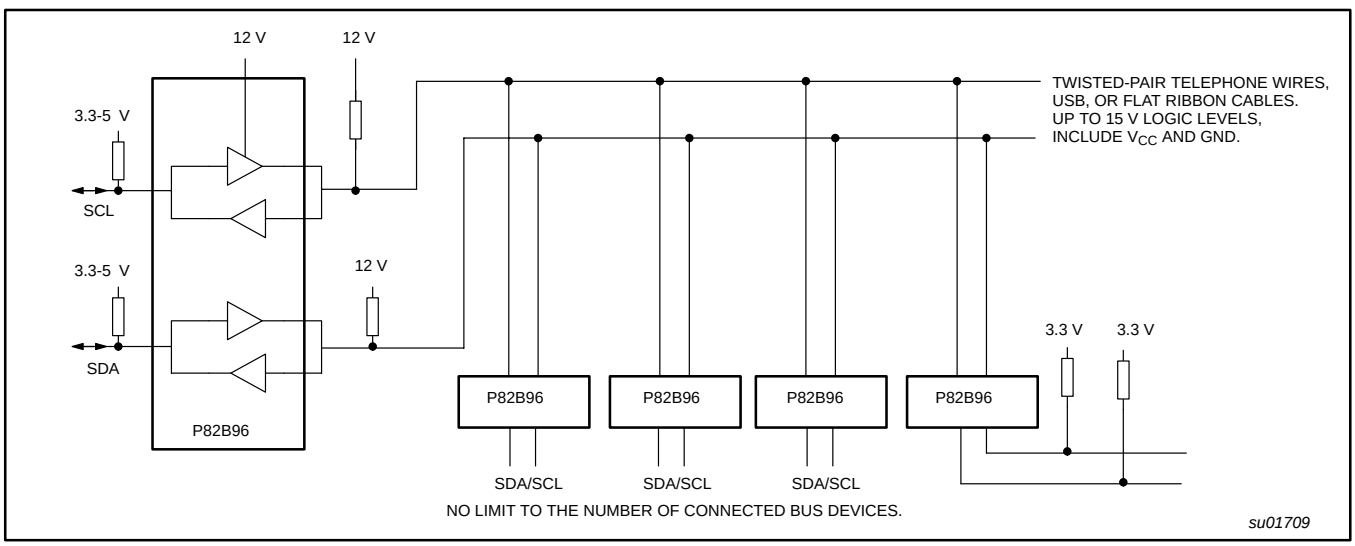


Figure 4. I²C multi-point applications

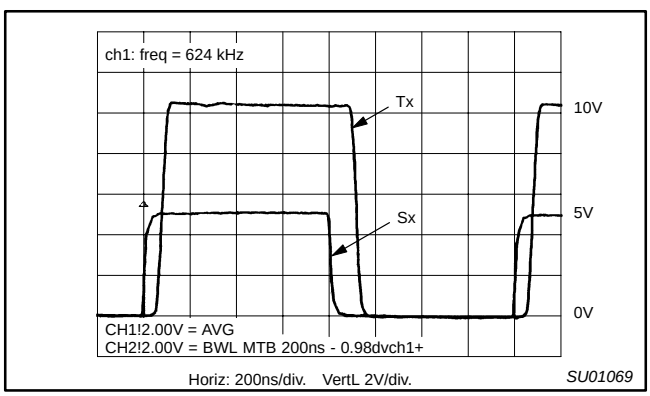


Figure 5. Propagation Sx to Tx — Sx pull-up to 5V, Tx pull-up to V_{CC} = 10 V

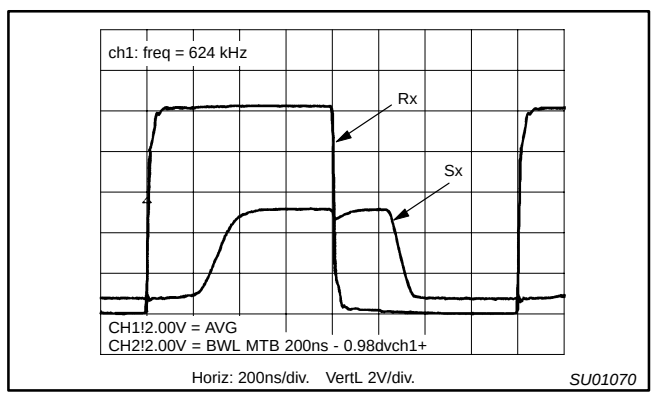
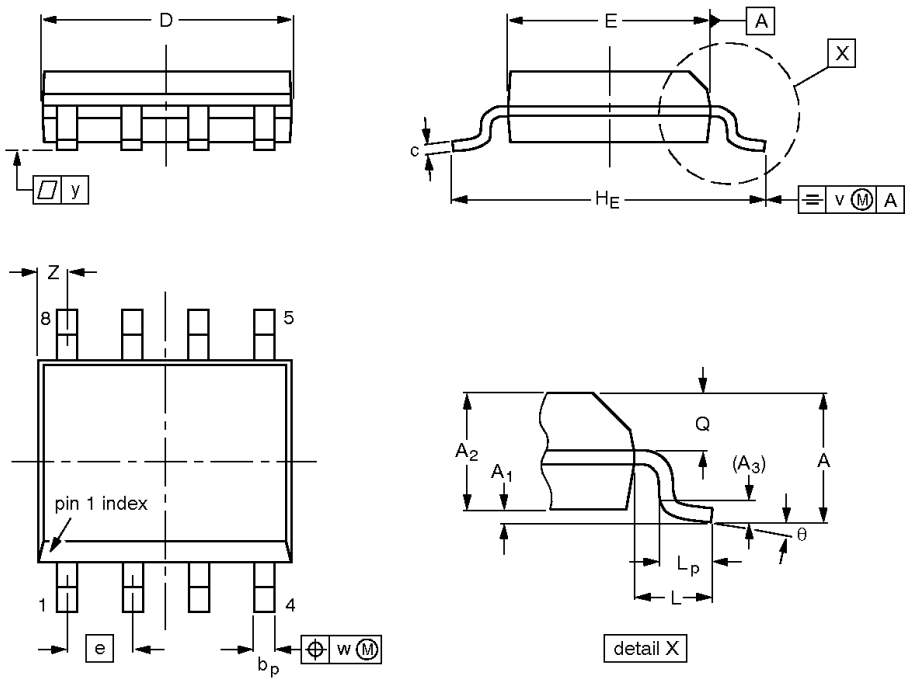
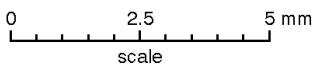


Figure 6. Propagation Rx to Sx — Sx pull-up to 5V, Rx pull-up to V_{CC} = 10 V

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

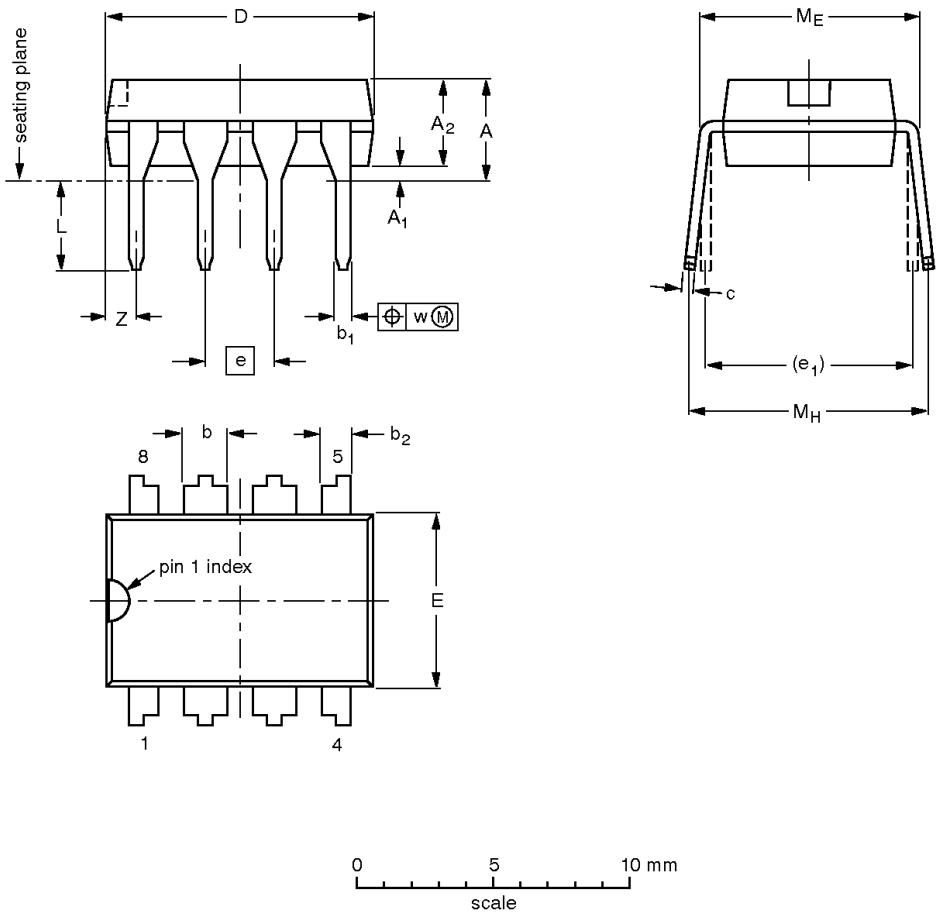
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03	MS-012				~~97-05-22~~ 99-12-27

DIP8: plastic dual in-line package; 8 leads (300 mil) **SOT97-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	$D^{(1)}$	$E^{(1)}$	e	e_1	L	M_E	M_H	w	$Z^{(1)}$ max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.020	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT97-1	050G01	MO-001	SC-504-8			~~95-02-04~~ 99-12-27

REVISION HISTORY

Rev	Date	Description
_3	20030402	**Product data (9397 750 11351); ECN 853-2241 29602 Dated 28 February 2003; supersedes data of 2003 Jan 22 (9397 750 11093)** Modifications: • Additional pin capacitance added.
_2	20030226	**Product data (9397 750 11093); ECN 853-2241 29410 of 22 January 2003; supersedes data of 2001 Mar 06 (9397 750 08122)**
_1	20010306	Product data (9397 750 08122); ECN 853-2241 25758 of 2001 Mar 06.

Dual bi-directional bus buffer P82B96

Data sheet status

Level	Data sheet status[1]	Product status[2] [3]	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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